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     FILE 'WPIX, JAPIO' ENTERED AT 12:01:30 ON 02 MAY 2002
L1          2210 S (SOLDERING OR SOLDERED OR SOLDER? OR SOLDER OR BRAZ?)(4N)(COL
L2           352 S (SOLDERING OR SOLDERED OR SOLDER? OR SOLDER OR BRAZ?) (4N)(MA
L3        660986 S (DIELECTRIC? OR OXIDE OR INSULAT?) (3N)(LAYER? OR MATERIAL? O
L4       4813769 S PACKAGE? OR ENCAS? OR PROTECT? OR CASING OR CASE OR CAVITY OR
L5         44820 S (CONTACT? OR BONDING OR CONNECT? OR JOIN?)(3N)(PAD OR PADS OR
L6           443 S (COLUMN OR FILE OR LINE OR QUEUE OR RANK OR ROW OR STRING OR
L7        848345 S IC OR ICS OR ((INTEGRATED OR LOGIC)(W)(CIRCUIT?)) OR (MICRO)(
L8        226577 S L7 AND L4
L9          7927 S L8 AND L5
L10           42 S L9 AND L1
L11            0 S L10 AND DISTAL
L12            6 S  L10 AND L3
L13          173 S (SOLDERING OR SOLDERED OR SOLDER? OR SOLDER OR BRAZ?)(4N)(COL
L14           73 S L13 AND L7
L15           15 S L14 AND L5
L16           13 S L15 NOT L12
L17       147739 S (PACKAGE? OR ENCAS? OR PROTECT? OR CASING OR CASE OR CAVITY O
L18            1 S L14 AND L17
L19            1 S L18 NOT (L16 OR L12)
L20            0 S L14 AND SHEETLIKE(3N)FLEXIBLE
L21            0 S L14 AND (SHEETLIKE OR SHEET(2N)LIKE)
L22            0 S L14 AND L2
L23            4 S L9 AND L2
L24            4 S L23 NOT (L16 OR L12 OR L19)

=> S L14 AND DISTAL
L25            0 L14 AND DISTAL
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L12 ANSWER 1 OF 6 WPIX (C) 2002 THOMSON DERWENT
AN 2002-082046 [11] WPIX
DNN N2002-061092 DNC C2002-024731
TI Electronic **package** for information handling systems, comprises circuitized substrate, thick planar heat sink, electrical conductors, first semiconductor **chip**, and second semiconductor **chip** coupled to first.
DC L03 U11
IN HORTON, R R; LANZETTA, A P; MILEWSKI, J M; MOK, L S; MONTOYE, R K; SHAUKATULLA, H
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 6326696 B1 20011204 (200211)* 11p
ADT US 6326696 B1 US 1998-18698 19980204
PRAI US 1998-18698 19980204
AB US 6326696 B UPAB: 20020215
NOVELTY - An electronic **package** comprises:
(i) a circuitized substrate with a **cavity** that passes through the substrate;
(ii) a thick planar heatsink having another **cavity**;
(iii) electrical conductors;
(iv) a first semiconductor **chip** in the **cavities**, directly connected to the conductors and thermally coupled to the heat sink; and
(v) a second semiconductor **chip** electrically coupled to the first semiconductor **chip**.
DETAILED DESCRIPTION - An electronic **package** comprises:
(a) a circuitized substrate (12) with a first and a second surface, and having a first **cavity** (14) that passes completely through the substrate;
(b) a thick planar heatsink (32) having a second **cavity**, and is bonded to the second surface of the substrate with the second **cavity** overlapping at least partially the first **cavity**;
(c) electrical conductors (24) positioned on the first surface of the circuitized substrate, and at least some are located about the periphery of the first **cavity**;
(d) a first semiconductor **chip** (16) positioned within the first and second **cavities**, directly electrically connected to at least some of the conductors and thermally coupled to the planar heatsink; and
(e) a second semiconductor **chip** which is positioned on and electrically coupled to the first semiconductor **chip**, and has an outer surface coplanar with the first surface of the substrate.
USE - For information handling systems (computer) field.
ADVANTAGE - The electronic **package** has at least two semiconductor **chips** that are electrically coupled, with one also electrically coupled to and positioned within a **cavity** in a substrate. The **package** also facilitates positioning the **chips** relative to **bonding pads** located on a first surface of the substrate. It is readily adapted for subsequent placement and coupling to a separate conductive substrate, i.e. printed circuit board.
DESCRIPTION OF DRAWING(S) - The figure shows a cross section of an electronic **package** where a heatsink is utilized.
Circuitized substrate 12
Cavity 14
First semiconductor **chip** 16
Electrical conductors 24

Heatsink 32
Dwg.2/6

L12 ANSWER 2 OF 6 WPIX (C) 2002 THOMSON DERWENT
AN 2001-233637 [24] WPIX
DNN N2001-166867
TI Small scale ball grid array **package** - improve the electrical performance and the heat dissipation efficiency.
DC U11
IN HE, T; HUANG, J; JIANG, W; CHIANG, K; HER, T; HUANG, C
PA (SILI-N) SILICONWARE PRECISION IND CO LTD
CYC 2
PI TW 409377 A 20001021 (200124)*
US 6218731 B1 20010417 (200129)
ADT TW 409377 A TW 1999-108359 19990521; US 6218731 B1 US 1999-383835 19990826
PRAI TW 1999-108359 19990521
AB TW 409377 A UPAB: 20010502
NOVELTY - A small scale ball grid array **package** is disclosed, which is formed on a substrate. The substrate is composed by stacking at least one **insulated layer** and at least two copper foil layers together. There is one void near the center of the substrate, and at least one second foil is allocated on one surface of the substrate. A plurality of electrical-conductive trace lines are formed by patterning, and another first copper foil, of which the surface is partly exposed, is electrical connected with the electrical-conductive trace through the through hole for grounding so as to form the grounding plane to improve the electrical performance and the heat dissipation efficiency of the **package**. A plurality of soldering pads are provided near the center of one surface of the **chip**. The surface is jointed with the grounding plane by heat conduction to make the soldering pad allocated in the void. The soldering **pad** is **connected** respectively with the proximity end of the electrical-conductive trace lines by one electrical-conduction wiring line. The far end of the electrical-conductive trace lines is linked respectively to one solder ball. The **package** material is filled in the void and covers the neighboring region of the void to **protect** the **soldering** pad, the wiring **line** and the electrical-conductive trace lines, and to cover the region where the **chip** and the grounding plane are jointed.
Dwg.0/0

L12 ANSWER 3 OF 6 WPIX (C) 2002 THOMSON DERWENT
AN 2001-121923 [13] WPIX
DNN N2001-089427
TI **Chip** scale **package** manufacturing method involves forming **solder column** at desired height by depositing and freezing one or more successive droplets on pads so that **pads** are electrically **connected**.
DC U11 X24
IN HAYES, D J
PA (MICR-N) MICROFAB TECHNOLOGIES INC
CYC 1
PI US 6114187 A 20000905 (200113)* 16p
ADT US 6114187 A Provisional US 1997-35305P 19970111, US 1998-4392 19980108
PRAI US 1997-35305P 19970111; US 1998-4392 19980108
AB US 6114187 A UPAB: 20010307
NOVELTY - The **microelectronic** device has array of inter **connected** metalized bond **pads** (2). A solder jetting nozzle jets droplets of molten solder towards individual interconnecting

pads on the **connection** surface, via an inert atmosphere. A **solder column** (3) is formed at desired height by depositing and freezing one or more successive droplets on the pads such that the **pads** are electrically **connected**.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **microelectronic package** manufacturing method.

USE - For high density **integrated circuits** e.g. **chip** scale **package**.

ADVANTAGE - Enables to perform very small **packages** not bigger than integrated **chip**, thereby cost is reduced. Certain amount of flexibility is added to electrical connection by **solder columns** that improves reliability of device.

DESCRIPTION OF DRAWING(S) - The figure shows cross-section through bare integrated **chip**, **row** of pads after **solder columns**, and figures showing embedded **solder column** and **dielectric coating** partially ablated away to expose the column ends.

Metalized bond pads 2

Solder column 3

2a, 2b, 2c, 2d/7

L12 ANSWER 4 OF 6 WPIX (C) 2002 THOMSON DERWENT
AN 2000-565141 [52] WPIX
DNN N2000-417428 DNC C2000-168285
TI Hermetically sealed photonic devices where photonic device is mounted on a transparent substrate, and hermetically sealed.
DC A85 L03 U11 U12 V08
IN ZHOU, P
PA (HONE) HONEYWELL INC
CYC 26
PI WO 2000041281 A1 20000713 (200052)* EN 31p
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: JP
EP 1145393 A1 20011017 (200169) EN
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
ADT WO 2000041281 A1 WO 1999-US27259 19991118; EP 1145393 A1 EP 1999-960433 19991118, WO 1999-US27259 19991118
FDT EP 1145393 A1 Based on WO 200041281
PRAI US 1998-224210 19981230
AB WO 200041281 A UPAB: 20001018

NOVELTY - A photonic device submount (100) comprises a photonic device (101) mounted on a substrate (102), and hermetically sealed (108).

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of hermetically sealing a photonic device, by forming the above structure.

USE - For photonic devices such as vertical **cavity** surface emitting lasers (VCSEL), used in the communications and electronic industries.

ADVANTAGE - Many hermetically sealed devices can be mass produced on **wafers**, unlike conventional methods typically using Kovar metal cans where only one device at a time can be sealed. A good seal is obtained.

DESCRIPTION OF DRAWING(S) - The drawing shows a side view of the photonic device submount.

Photonic device 101

Substrate 102

Signal lines 104

Dielectric layer 106

Hermetic seal 108
Lift-off layer 110
Bonding pad 112
Metal layer 206
Dwg.2/14

L12 ANSWER 5 OF 6 WPIX (C) 2002 THOMSON DERWENT
AN 1992-383361 [47] WPIX
DNN N1992-292309 DNC C1992-170057
TI Semiconductor **package** e.g. lead-on-**chip**, small outline J-lead type - has **chip** with several solder points which are **soldered** to numerous inner **lines** of conductor frame.
DC A85 L03 U11 U14
IN CHA, G B
PA (GLDS) GOLDSTAR ELECTRON CO LTD; (KINS-N) KINSEI ELECTRON KK; (GLDS) GOLDSTAR CO LTD
CYC 5
PI DE 4215471 A 19921112 (199247)* 9p
JP 05136202 A 19930601 (199326) 5p
TW 221522 A 19940301 (199416)
US 5334873 A 19940802 (199430) 9p
KR 9406164 B1 19940708 (199616)
ADT DE 4215471 A DE 1992-4215471 19920511; JP 05136202 A JP 1992-114939 19920507; TW 221522 A TW 1992-102561 19920402; US 5334873 A US 1992-872154 19920422; KR 9406164 B1 KR 1991-7631 19910511
PRAI KR 1991-7631 19910511
AB DE 4215471 A UPAB: 19931006
The semiconductor **chip** in the **package** has a number of **soldering** points on its plastics **lines**. There are numerous inner **lines** of a conductive frame, **soldered** to the points, which may be of Pb-Sn alloy etc. whose melting temp. is higher than that of the epoxy hardening temp.

Each soldering point is typically spherical, with the plastics lines of the **chip** set along a longitudinal line. Alternatively they are arranged along two such lines. They may be also of zigzag shape. In the mfg., polyimide films are formed on the semiconductor **chip** surface, and the soldering points are formed on each plastics line.

USE/ADVANTAGE - Also for MSP, QFP-type **packages**, e.g. for memory **integrated circuit chips**, with improved design reduced **package** thickness, without using wire bonding process.
3/6

L12 ANSWER 6 OF 6 JAPIO COPYRIGHT 2002 JPO
AN 1986-036962 JAPIO
TI **PACKAGE** FOR ELECTRONIC CIRCUIT
IN NAKAKITA SHOJI
PA NEC CORP, JP (CO 000423)
PI JP 61036962 A 19860221 Showa
AI JP1984-159833 (JP59159833 Showa) 19840730
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 417, Vol. 1, No. 192, P. 93 (19860705)
AB PURPOSE: To improve yield, to reduce cost and to enhance reliability on quality by combining a high-temperature baked substrate with a common power-supply wiring circuit and a low-temperature baked substrate with a signal wiring circuit by solder.
CONSTITUTION: A high-temperature baked substrate 1 has a power-supply wiring circuit 11, pin pads 12, **pads** 13 for **connection** and through holes 14. On the other hand, a low-temperature baked substrate

2 has **pads** 21 for **connection** and through holes 22, and **integrated circuits** 5 are mounted onto the upper surface of the substrate 2 through an **insulating layer** section 24. The **pads** 13, 21 for **connecting** each substrate 1, 2 are connected electrically and mechanically through **solder** 4. Accordingly, when signal **line** patterns in the substrate 2 and the **integrated circuits** 5 get trouble, both substrates 1, 2 are separated by melting **solder** 4, and these signal **line** patterns and **integrated circuits** can be exchanged with acceptables.

L16 ANSWER 1 OF 13 WPIX (C) 2002 THOMSON DERWENT
AN 2001-090493 [10] WPIX
CR 1999-560763 [47]
DNN N2001-068543 DNC C2001-026454
TI Connection of two electronic objects involves placing solder **bump** on first **bonding pad** and second **bonding pad** on the solder bump, and heating the solder bump.
DC L03 U11 V04
IN GALLOWAY, T R
PA (INTE-N) INTEGRATED DEVICE TECHNOLOGY
CYC 1
PI US 6166334 A 20001226 (200110)* 9p
ADT US 6166334 A Div ex US 1997-781740 19970110, US 1999-287549 19990406
FDT US 6166334 A Div ex US 5957370
PRAI US 1997-781740 19970110; US 1999-287549 19990406
AB US 6166334 A UPAB: 20010220
NOVELTY - Electronic objects are connected by placing a solder bump on a first object **bonding pad** with continuous planar surface and a second object **bonding pad** on the solder bump, and heating the solder bump to form an hourlyglass-shaped **solder column** electrically coupling the objects. The solder bump has a C-shaped annular cylinder of solder material surrounding an inner cylinder of a lower density.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for an intermediate structure for use in connecting electronic components comprising a **bonding pad** (105), a barrier metal layer (215), and a solder bump.

USE - For connecting two electronic objects.

ADVANTAGE - The solder bumps has a maximum width not appreciably greater than the diameter of the **bonding pad** that allows finer pitch **die** in **wafer** form. The invention allows higher packing densities that are effectively limited by the **bonding pad** and not the geometry of the solder bump. It achieves smaller pitches than in prior art and allows a higher density of **bonding pads** which gives more pin outs from a **chip** that is important in multimedia **chips** and microprocessor telecommunication **chips**. The plated solder bumps possess a cylindrical shape with an aspect ratio approaching 1 as opposed to the mushroom shape produced using the conventional processes.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of an interconnection on a semiconductor device.

Bonding pad 105
Solder bump 120
Barrier metal layer 215
Dwg.2/5

L16 ANSWER 2 OF 13 WPIX (C) 2002 THOMSON DERWENT
AN 2000-364383 [31] WPIX
CR 2002-215037 [14]
DNN N2000-272712 DNC C2000-109856
TI Microgrid array solder interconnect structure, has microgrid array of solder connections for **joining** solder wettable **pads** of **chip** carrier and printed circuit board.
DC L03 P55 V04 X24
IN MAYS, A T; SLESINGER, K A; WELLER, M C
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 6059173 A 20000509 (200031)* 4p

ADT US 6059173 A US 1998-35538 19980305
PRAI US 1998-35538 19980305
AB US 6059173 A UPAB: 20020429
NOVELTY - **Solder columns** (3) which interconnect **chip** carrier (1) and printed circuit board (2), are formed by solder connections arranged in microgrid array. The **solder columns join solder** wettable **pads** on main surface of **chip** carrier corresponding to that of printed circuit board.

DETAILED DESCRIPTION - The **solder** connections are **column** shaped with specific height and diameter. The **chip** carrier comprises ceramic substrate or alternatively organic polymer substrate.

USE - For interconnecting electronic array module and printed circuit module.

ADVANTAGE - Solder connections are non-collapsible at fabrication temperature and exhibit reduced stress by providing correct thermal matching of **chip** carrier and PCB.

DESCRIPTION OF DRAWING(S) - The figure shows the schematic diagram of solder.

Chip carrier 1
Printed circuit board 2
Solder columns 3

Dwg.1/1

L16 ANSWER 3 OF 13 WPIX (C) 2002 THOMSON DERWENT
AN 2000-364087 [31] WPIX
DNN N2000-272425
TI **Integrated circuit** with programmable substrate for array type packages, has electrical and mechanical connectors to connect via on bottom of substrate to printed circuit board.
DC U11
IN CHIA, C J; LIM, S; VARIOT, P
PA (LSIL-N) LSI LOGIC CORP
CYC 1
PI US 6054767 A 20000425 (200031)* 8p
ADT US 6054767 A US 1998-6584 19980113
PRAI US 1998-6584 19980113
AB US 6054767 A UPAB: 20000630
NOVELTY - The programmable substrate (12) has a mounting area to mount an **IC die**. Multiple electrically conductive vias (22) passes between top and bottom of the substrate. A via bond wire (34) selectively connects electrical trace which are formed on top of substrate, to different vias. Electrical and mechanical connectors connects vias on the bottom of the substrate to a printed circuit board.

DETAILED DESCRIPTION - The electrical and mechanical connector comprises array of **solder** balls, **columns**, pins.

USE - For array type packages including Ball Grid Arrays (BGA), Pin Grid Arrays (PGA) and Column Grid Arrays (CGA).

ADVANTAGE - Since the substrate can be programmed or easily reused or modified by the assembly manufacturer to allow **pad**-to-pin **connections**, the fabrication cycle time for new designs is reduced and therefore design and implementations of different **IC** packages becomes more cost effect. The compatibility of the programmable substrate with wide variety of **integrated circuits** is improved.

DESCRIPTION OF DRAWING(S) - The figure shows cross sectional view of **integrated circuit** package.

Programmable substrate 12

Electrically conductive vias 22
Via bond wire 34
Dwg.3/3

L16 ANSWER 4 OF 13 WPIX (C) 2002 THOMSON DERWENT
AN 1999-560763 [47] WPIX
DNN N1999-414311 DNC C1999-163355
TI Plating process for making solder interconnections on **integrated circuit**.
DC L03 P55 U11
IN GALLOWAY, T R
PA (INTE-N) INTEGRATED DEVICE TECHNOLOGY
CYC 1
PI US 5957370 A 19990928 (199947)* 9p
ADT US 5957370 A US 1997-781740 19970110
PRAI US 1997-781740 19970110
AB US 5957370 A UPAB: 20010220
NOVELTY - A solder interconnection (120) between two **bonding pads** (130) is formed by creating an apertured tape over one pad, filling the aperture with solder and **connecting** the second **pad**.
DETAILED DESCRIPTION - Making solder interconnections on an **integrated circuit** comprises applying a tape layer to a **die** surface (125) having a **bonding pad** (130), forming an aperture in the tape to the pad, filling this with solder and removing the tape. A second **bonding pad** is aligned with the solder and first **pad**, **contacted** with the solder **bump** (120) and heated to form a connecting **solder column**.
USE - In interconnecting **bonding pads** in **integrated circuits** (claimed).
ADVANTAGE - Packing density is increased since the solder bumps have similar widths to the **bonding pads** and smaller pitches can be used.
DESCRIPTION OF DRAWING(S) - The alignment of solder **bump** and **bonding pad** is shown.
Solder bump 120
Die 125
Bonding pad 130
Dwg.1f/5

L16 ANSWER 5 OF 13 WPIX (C) 2002 THOMSON DERWENT
AN 1999-264424 [23] WPIX
DNN N2000-135278 DNC C2000-057651
TI Solder structure for bonding electronic substrates comprises a **column** of tin-lead **solder** which has at its free end a layer of a metal forming a single phase ternary alloy with the solder upon reflow.
DC L03 M23 P55 U11
IN DIGIACOMO, G
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 5
PI CN 1205927 A 19990127 (199923)* 1p
KR 99013414 A 19990225 (200017)
US 6025649 A 20000215 (200017)B 9p
SG 74641 A1 20000822 (200049)
US 6196443 B1 20010306 (200115)
TW 411744 A 20001111 (200121)
US 6329721 B1 20011211 (200204)

ADT CN 1205927 A CN 1998-114952 19980622; KR 99013414 A KR 1998-22221 19980613; US 6025649 A US 1997-898443 19970722; SG 74641 A1 SG 1998-1810 19980716; US 6196443 B1 Div ex US 1997-898443 19970722, US 1998-118117 19980716; TW 411744 A TW 1998-103419 19980309; US 6329721 B1 Div ex US 1997-898443 19970722, Div ex US 1998-118117 19980716, US 2000-570884 20000515

FDT US 6196443 B1 Div ex US 6025649; US 6329721 B1 Div ex US 6025649, Div ex US 6196443

PRAI US 1997-898443 19970722; US 1998-118117 19980716; US 2000-570884 20000515

AB US 6025649 A UPAB: 20000405 ABEQ treated as Basic

NOVELTY - The **solder column** is connected at its **solder** end to **pads** or **bonding** sites on a first substrate. When it is connected at the metal layer end by reflow to a second substrate, the ternary alloy is formed in which the ratio of lead to tin is about the same as in the solder.

DETAILED DESCRIPTION - The solder preferably comprises 3wt% Sn, balance Pb. The metal layer is preferably In.

USE - In fabrication of packaged components by Controlled Collapse **Chip** Connection technology.

ADVANTAGE - A solder bond is formed having enhanced fatigue resistance.

DESCRIPTION OF DRAWING(S) - The drawings show a **solder column** connection of the invention and a graph of ternary alloy joint thickness after reflow versus reflow temperature for various In layer thicknesses.

First and second substrates 11,20

Solder column 22

Contact pads 14,23

Ternary alloy joint formed following reflow 21

Dwg.1E,3/3

AB CN 1205927 A UPAB: 20000412

NOVELTY - The **solder column** is connected at its **solder** end to **pads** or **bonding** sites on a first substrate. When it is connected at the metal layer end by reflow to a second substrate, the ternary alloy is formed in which the ratio of lead to tin is about the same as in the solder.

DETAILED DESCRIPTION - The solder preferably comprises 3wt% Sn, balance Pb. The metal layer is preferably In.

USE - In fabrication of packaged components by Controlled Collapse **Chip** Connection technology.

ADVANTAGE - A solder bond is formed having enhanced fatigue resistance.

DESCRIPTION OF DRAWING(S) - The drawings show a **solder column** connection of the invention and a graph of ternary alloy joint thickness after reflow versus reflow temperature for various In layer thicknesses.

First and second substrates 11,20

Solder column 22

Contact pads 14,23

Ternary alloy joint formed following reflow 21

Dwg.1E,3/3

L16 ANSWER 6 OF 13 WPIX (C) 2002 THOMSON DERWENT

AN 1998-148103 [14] WPIX

DNN N1998-117387

TI Copper column contact for flexible circuit - has raised features as part of electrical traces, with barrier metallisation layer, on flexible circuit, with features **connected** to **chip**

contact pads via solder **bump**.

DC U11
IN LE, B; SCHREIBER, C M
PA (PACB) PACKARD HUGHES INTERCONNECT CO
CYC 3
PI GB 2317268 A 19980318 (199814)* 12p
DE 19738158 A1 19980326 (199818) 5p
US 5790377 A 19980804 (199838)
GB 2317268 B 19981028 (199845)
ADT GB 2317268 A GB 1997-16867 19970811; DE 19738158 A1 DE 1997-19738158 19970901; US 5790377 A US 1996-713084 19960912; GB 2317268 B GB 1997-16867 19970811
PRAI US 1996-713084 19960912
AB GB 2317268 A UPAB: 19980406
The flexible circuit (14) includes several electrical traces (20) which include raised features (16,18). The electrical traces and raised features are made of copper. An **integrated circuit chip** has an electrical circuit with a **contact pad** (12). There is a barrier metallisation layer (13) over the **contact pad** and solder (26) extends between the metallisation layer and the raised feature to define an integral copper **column** with **solder** bump flip **chip** (10).

The raised feature and solder has a combined height of between 6 and 12 mils, and the solder has a height of between 4 and 6 mils. The raised feature and solder provide electrical connection between the **integrated circuit chip** and the circuit on the flex circuit, or they are isolated from the circuit on the flex circuit and provide a heat sink path for heat from the **integrated circuit**. A multichip module underlies the flex circuit and is electrically connected to it.

ADVANTAGE - Increases height that flip **chip** can be raised off substrate without increasing area of substrate or **chip** used.
Dwg.1/1

L16 ANSWER 7 OF 13 WPIX (C) 2002 THOMSON DERWENT
AN 1997-448043 [41] WPIX
DNN N1997-373405
TI Ball grid array package with lead frame - has lead frame structure in place of substrate, and includes **die** attachment **pad** electrically **connected** to leads by wire bonding.
DC U11
IN MOSTAFAZADEH, S; SMITH, J O
PA (NASC) NAT SEMICONDUCTOR CORP
CYC 1
PI US 5663593 A 19970902 (199741)* 6p
ADT US 5663593 A US 1995-543978 19951017
PRAI US 1995-543978 19951017
AB US 5663593 A UPAB: 19971013
The package includes a lead frame that includes **die** attaching pad and a number of leads radiating from the **die** attaching pad. The **die** is mounted on the **die** attaching **pad** and electrically **connected** to the leads by wire bonding.

A non-conductive solder mask or tape is applied to the lead frame which defines a number of selected positioned vias. A moulded plastic casing or cap is positioned over the **die**, wiring and lead frame to encapsulate the package. **Solder** balls or **columns** are attached to selected leads of the frame through the vias.

ADVANTAGE - Exhibits reduction in manufacturing cost while

maintaining small footprint.
Dwg.7/7

L16 ANSWER 8 OF 13 WPIX (C) 2002 THOMSON DERWENT
AN 1997-341042 [31] WPIX
CR 1996-370098 [37]
DNN N1997-283004 DNC C1997-109534
TI Reliable electronic package and **integrated circuit** board connection - using laminated **solder column** attached to electrical **contact pads** with high and low melting point solder layers to retain stability.
DC L03 M23 U11
IN CHIU, G W
PA (ITLC) INTEL CORP
CYC 1
PI US 5641990 A 19970624 (199731)* 7p
ADT US 5641990 A Div ex US 1994-307893 19940915, US 1995-512024 19950807
FDT US 5641990 A Div ex US 5542174
PRAI US 1994-307893 19940915; US 1995-512024 19950807
AB US 5641990 A UPAB: 19970731
Electrical/mechanical connection between an electronic package and a printed circuit board comprise a) a substrate (30) with first surface, b) electrical **contact pads** (34) on first surface and, c) a laminated **solder column** attached to the electrical **contact pads** comprising a first and second thinner solder layer, the second layer is coupled to one of the electrical **contact pads** with a melting temperature below the melting pt. of the first layer.

Also claimed is an electronic package with three solder layers separated by two barrier layers, the first (32b) and second (31) solder layers are separated by the first barrier (33b) and the second (31) and third (32a) solder layers by the second barrier (33a ; the first and third solder layers are thinner than that of the second solder layer and having a lower melting temperature than the second solder layer. The third layer is attached to the **contact pads** and on reflow forming a column grid array.

USE - For improved column grid arrays and ball grid arrays for connecting packages to printed circuit boards.

ADVANTAGE - An improved ball grid array (i) that avoids the positioning problems associated with the prior art, reducing the cost of manufacture as less flux is required and uniformity is easier to control. The improved column grid array (ii) uses a central high melting point portion that prevents column collapse during reflow melting, ensuring a reliable electrical/mechanical connection.
Dwg.4A/5

L16 ANSWER 9 OF 13 WPIX (C) 2002 THOMSON DERWENT
AN 1997-322499 [30] WPIX
DNN N1997-266862
TI Plastic packaging of surface mounted **integrated circuit** packages e.g. ball grid arrays - comprises package including circuit enclosed by plastic body, conductive pads are adjacent to openings package through which conductors **connected** to **pads** extend.
DC U11
IN ABBOTT, J A; KALIDAS, N; THOMPSON, R W; ABBOTT, J H
PA (TEXI) TEXAS INSTR INC
CYC 8
PI EP 780896 A2 19970625 (199730)* EN 8p
R: DE FR GB IT NL

JP 09191060 A 19970722 (199739) 5p
US 5777382 A 19980707 (199834)
SG 52875 A1 19980928 (199904)
US 5976914 A 19991102 (199953)#
ADT EP 780896 A2 EP 1996-309224 19961218; JP 09191060 A JP 1996-339174 19961219; US 5777382 A Provisional US 1995-8899P 19951219, US 1996-769917 19961219; SG 52875 A1 SG 1996-11856 19961219; US 5976914 A Div ex US 1996-769917 19961219, US 1997-918404 19970826
FDT US 5976914 A Div ex US 5777382
PRAI US 1995-8899P 19951219; US 1996-769917 19961219; US 1997-918404 19970826
AB EP 780896 A UPAB: 19970723
The moulded plastic body (12,14) encloses an electronic circuit and a lead frame comprising lead fingers. Conductive strips are electrically connected to the circuit contacting one surface of the body. The surface of the package (10) includes openings (22) adjacent to conductive pads (18). The conductive **pads** are **connected** to the strips.
Conductors, which extend outwards through the openings are **connected** to the **pads**. The conductors comprise either conductive **solder** balls **columns** or pins.
ADVANTAGE - robust, reduces difficulty in manufacturing, cost-effective, easy access for testing.
Dwg.1/4

L16 ANSWER 10 OF 13 WPIX (C) 2002 THOMSON DERWENT
AN 1992-086549 [11] WPIX
DNN N1992-064744 DNC C1992-040221
TI Encapsulated, cleavable, controlled collapse **chip** connections - having circuitry built in and **connection pads** with high m.pt. **solder columns** etc..
DC A85 L03 M23 R46 U11
PA (ANON) ANONYMOUS
CYC 1
PI RD 334086 A 19920210 (199211)* 1p
PRAI RD 1992-334086 19920120
AB RD 334086 A UPAB: 19931006
The semiconductor **chips** (11) have circuitry built in and have **connection pads** on which the high-m pt. **solder columns** (13) reside. The **solder columns** (13) are surrounded by a layer of encapsulant (12). The **solder columns** could be 97Pb-3Sn and the encapsulant could be Upilex or Xyder. Layers of interface metals are added between the **solder columns** and **chip connection pads**.
The solder balls (14) are placed under the **solder columns** (13). They are made of relatively low-m pt. solder such as eutectic Pb/Sn solder. The solder balls (14) are bonded on the **connection pads** (15) on the substrate (16). The solder balls (14) are not encapsulated so that they can be reworked or repaired with conventional methods.
1/1

L16 ANSWER 11 OF 13 WPIX (C) 2002 THOMSON DERWENT
AN 1988-115927 [17] WPIX
TI Soldering flip **chip** onto circuit board - by forming **column** shaped **soldering bump** giving good **connection** NoAbstract Dwg 1a-d/4.
DC L03 U11 U14
PA (OKID) OKI ELECTRIC IND CO LTD
CYC 1

PI JP 63062333 A 19880318 (198817)* 5p
ADT JP 63062333 A JP 1986-206025 19860903
PRAI JP 1986-206025 19860903

L16 ANSWER 12 OF 13 JAPIO COPYRIGHT 2002 JPO
AN 1990-100353 JAPIO
TI SEMICONDUCTOR DEVICE
IN KATO CHIKAYUKI; NISHINO SEIICHI; YAMADA JIRO
PA NEC CORP, JP (CO 000423)
NEC ENG LTD, JP (CO 329822)
PI JP 02100353 A 19900412 Heisei
AI JP1988-254234 (JP63254234 Heisei) 19881007
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 947, Vol. 14, No. 3, P. 130 (19900703)
AB PURPOSE: To make a device smaller and light by increasing the ratio accounting for the area of a **die** pad to the surface of a wiring board with the foregoing area kept constant and then, disposing input/output **pads** for external **connection** that are about the same number as those which are obtained before the ratio accounting for the above area to the surface of the wiring board increases in such a way that they are arrayed in a staggered lattice or in a parallel lattice.
CONSTITUTION: This device makes the ratio accounting for the area of a **die** pad to the surface of a wiring board increase with the foregoing area kept constant. Input/output **pads** for external **connection** that are around the same number as those which are obtained before the ratio accounting for the above area to the surface of the wiring board increases are disposed in such a way that they are arrayed in a staggered lattice or in a parallel lattice. For example, in addition to forming a wiring circuit on the surface of an insulating substrate 1, in an external connection part, the input/output **pads** 2 for external **connection** allow 72 pins to be formed into three **columns** by a **solder** DIP system and the like. In other words, in the case where respective pins formed into three columns are put in the same file, each pitch becomes 2.54mm. As an intermediate column is slid at a distance of 1.27mm, pins are formed, on the whole, into a staggered lattice and then its staggered direction is made up so that are 1.27.times.2mm pitches. A package is thus made smaller and lighter than that having the pitches 2.54mm.

L16 ANSWER 13 OF 13 JAPIO COPYRIGHT 2002 JPO
AN 1980-043811 JAPIO
TI SEMICONDUCTOR **INTEGRATED CIRCUIT** DEVICE
IN OSHIMA MUNEO; NAKAMURA MASANORI
PA HITACHI LTD, JP (CO 000510)
PI JP 55043811 A 19800327 Showa
AI JP1978-115787 (JP53115787 Showa) 19780922
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 13, Vol. 4, No. 751, P. 75 (19800531)
AB PURPOSE: To prolong fatigue breakage life due to repetitive displasement by controlling shape of a solder bump surrounding tip for electrical **connection** by a **bump** in the tip's center section.
CONSTITUTION: By changing size of solder bumps on an **IC** tip 1, respectively required volumes of bumps are achieved on an electrode 2 and a control electrode 11. On a base board on which pedestals are formed in positions corresponding to the electrode 2 and the control electrode 11, positioning is made with face down and heated to melt for completion of connection. As a **solder column** 9 is to have stretched connection intervals due to a **solder column** 10 if the

control section, its fatigue breakage life can be prolonged.

L19 ANSWER 1 OF 1 WPIX (C) 2002 THOMSON DERWENT
AN 1987-309722 [44] WPIX
TI LSI **chip** carrier without wire bonding portion - has **solder columns**, formed through **insulative protective** film on LSI **chip** NoAbstract Dwg 1/5.
DC U11 U14
PA (HITA) HITACHI LTD
CYC 1
PI JP 62217620 A 19870925 (198744)* 4p
ADT JP 62217620 A JP 1986-59213 19860319
PRAI JP 1986-59213 19860319

L24 ANSWER 1 OF 4 WPIX (C) 2002 THOMSON DERWENT
AN 2002-126371 [17] WPIX
DNN N2002-094820
TI Flip-**chip** mounting method for **integrated circuit chip**, involves **connecting** solder **bump** of **chip** and electrode of wiring board after mounting solder bump whose surface is reformed on electrode.
DC U11 V04 X24
PA (TAKX) TAMURA SEISAKUSHO KK
CYC 1
PI JP 2001308144 A 20011102 (200217)* 8p
ADT JP 2001308144 A JP 2000-124508 20000425
PRAI JP 2000-124508 20000425
AB JP2001308144 A UPAB: 20020313
NOVELTY - The surface of the lead free tin-zinc group **solder** bump (12) **containing** 10 % **mass** of bismuth, indium and copper of an **integrated circuit** (**IC**) **chip** (11) is reformed. The reformed bump is mounted on the metal electrode of a wiring board directly, and connected to the electrode.
USE - For flip-**chip** mounting of the solder terminal of the **integrated circuit chip** on a wiring board using controlled collapse **chip** connection.
ADVANTAGE - By reforming the solder surface, the connection reliability between the terminals is improved without using a flux, thereby eliminates the post-cleaning process of flux.
DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of plasma processing in flip-**chip** mounting method. (Drawing includes non-English language text).
IC chip 11
Solder bump 12
Dwg.1/4

L24 ANSWER 2 OF 4 WPIX (C) 2002 THOMSON DERWENT
AN 1998-232888 [21] WPIX
DNN N1998-184523
TI Wired board with improved **bonding pads** - has interconnecting conductors used as ball grid array **package** base for **integrated circuit packages** and resinous printed substrate board, adapted to mount BGA **package** base.
DC U11 U14
IN SAKAI, H; YAMSAKI, K; SAIKI, H; YAMASAKI, K
PA (NITS) NGK SPARK PLUG CO LTD
CYC 25
PI EP 838854 A2 19980429 (199821)* EN 16p
R: AL AT BE CH DE DK ES FI FR GB GR IE IT LI LT LU LV MC NL PT RO SE SI
JP 10135613 A 19980522 (199831) 8p
US 6018197 A 20000125 (200012)
ADT EP 838854 A2 EP 1997-118637 19971027; JP 10135613 A JP 1996-303967 19961028; US 6018197 A US 1997-958083 19971027
PRAI JP 1996-303967 19961028
AB EP 838854 A UPAB: 19980528
The wired board comprises a substrate made of an insulation material and having a main surface, and a number of **bonding pads** disposed on the main surface of the substrate, each **bonding pad** having an integral axial projection. The substrate has a main surface, and the **bonding pads** each has a solderable outer surface, disposed on the main surface of the substrate.

Each of the **bonding pads** has a projection having a solderable outer surface and positioned inside an outer periphery when observed in a plan view. The projection comprises a ceramic body and a metallic layer formed on an outer surface of the ceramic body.

Each **bonding pad** is bonded to a solder ball by solder which is lower in melting point than the solder ball. The ceramic board and a resinous printed board are placed one upon another in such a manner that their **bonding pads** are aligned with each other. The **bonding pads** are soldered together with low melting point solder. The projection of each **bonding pad** is embedded in or surrounded by a **mass** of low melting point **solder** and joined with the **mass** of **solder** to constitute an integral unit while serving as a core of the unit.

ADVANTAGE - Prevents initiation and growth of crack or cracks in **masses** of **solder** for **connecting** between **bonding pads** of mating wired board.

Dwg.7/18

L24 ANSWER 3 OF 4 WPIX (C) 2002 THOMSON DERWENT
AN 1992-024644 [03] WPIX
TI Elongated **solder** interconnection - comprising a **solder mass encapsulated** by electrically conductive material and capped with a second **solder mass**.
DC L03 U11 U14
IN AGARWALA, B N; AHSAN, A M; BROSS, A; CHADURJIAN, M F; KOOPMAN, N G; LEE, L; PUTTLITZ, K J; RAY, S K; RYAN, J G; SCHAEFER, J G; SRIVASTAVA, K K; TOTTA, P A; WALTON, E G; WIRSING, A E; LEE, L C
PA (IBMC) INT BUSINESS MACHINES CORP; (IBMC) IBM CORP
CYC 17
PI WO 9120095 A 19911226 (199203)*
RW: AT BE CH DE DK ES FR GB IT LU NL SE
W: BR CA JP
US 5130779 A 19920714 (199231) 15p
EP 540522 A1 19930512 (199319) EN 59p
R: BE CH DE DK ES FR GB IT LI NL SE
US 5251806 A 19931012 (199342) 16p
JP 05507174 W 19931014 (199346) 16p
CA 2084685 C 19960116 (199614)
ADT US 5130779 A US 1990-540256 19900619; EP 540522 A1 WO 1990-US5931 19901016, EP 1991-905975 19901016; US 5251806 A Div ex US 1990-540256 19900619, US 1992-870647 19920416; JP 05507174 W WO 1990-US5931 19901016, JP 1991-505930 19901016; CA 2084685 C CA 1990-2084685 19901016
FDT EP 540522 A1 Based on WO 9120095; US 5251806 A Div ex US 5130779; JP 05507174 W Based on WO 9120095
PRAI US 1990-540256 19900619
AB WO 9120095 A UPAB: 19931006
A solder interconnection is claimed and comprises: a) a site for a **solder mass**, b) a **solder mass** formed on said site, and c) a material substantially **encapsulating** the **solder mass**.

More specifically, the side for the **solder mass** is on an active electronic component, partic. a **chip**, or a passive electronic component, partic. a substrate. USE/ADVANTAGE - Used for solder interconnections for electronic components at high mounting density in LSI circuits. Allows the reliability of controlled coallpse **chip connection** (c4) **pads** to be improved by providing a means to increase the **chip** to substrate height. @ 4/17@

L24 ANSWER 4 OF 4 WPIX (C) 2002 THOMSON DERWENT
AN 1991-272037 [37] WPIX
DNN N1991-207522
TI Interposer approach to **chip**-to-carrier wire bonding - adding pedestal of pure gold to **pad** by ball **bonding** and flattening, so providing stress isolation.
DC U11
PA (ANON) ANONYMOUS
CYC 1
PI RD 328078 A 19910810 (199137)*
PRAI RD 1991-328078 19910720
AB RD 328078 A UPAB: 19930928
A bonding pedestal is added to those sites that require to be bonded. Depending on the number of such sites, two approaches can be used. If all or a large number of pads are involved, one would use a gang addition approach where pedestals are placed on all the pads and attached by a **soldering** or **brazing** process en **masse**. The pedestal material in this **case** can be selected to provide thermal expansion match to the substrate and stress relief during bonding, in addition to providing a bondable surface.

In **cases** where the bonding is needed only at a few pad sites, one can add a pedestal of pure Au by Au ball **bonding** to the **pad** and flattening to achieve a pedestal of several tens of microns in thickness. In either **case**, the pedestals provide an isolation of the substrate from the stresses of bonding as well as wire removal and repair.

ADVANTAGE - Relaxes requirements of thickness and adhesion levels of metallurgy of pads on substrate itself and allow relaxed toughness requirements on substrate.

FILE 'WPIX, JAPIO' ENTERED

L1 2213 S (SOLDERING OR SOLDERED OR SOLDER? OR SOLDER OR BRAZ?) (4N)(COLUMN OR FILE OR LINE OR QUEUE OR RANK OR ROW OR STRING OR TIER OR MATRIX OR DETERMINANT)

L2 354 S (SOLDERING OR SOLDERED OR SOLDER? OR SOLDER OR BRAZ?) (4N)(MASS##)

L3 661632 S (DIELECTRIC? OR OXIDE OR INSULAT?) (3N)(LAYER? OR MATERIAL? OR FILM? OR COAT#### OR MATERIAL OR ELEMENT OR MULTILAYER? OR MULTI(W) LAYER?)

L4 4816224 S PACKAGE? OR ENCAS? OR PROTECT? OR CASING OR CASE OR CAVITY OR ENCAPSULAT? OR CAPSUL? OR CASE OR CONTAIN? OR JACKET?

L5 44917 S (CONTACT? OR BONDING OR CONNECT? OR JOIN?)(3N)(PAD OR PADS OR BUMP OR BUMPS)

L6 443 S (COLUMN OR FILE OR LINE OR QUEUE OR RANK OR ROW OR STRING OR TIER OR MATRIX OR DETERMINANT)(4N)(INCLUSIO N?)

L7 863271 S IC OR ICS OR ((INTEGRATED OR LOGIC)(W)(CIRCUIT?)) OR (MICRO)(W)(CIRCUIT? OR CHIP OR ELECTRONIC?) OR CHIP? OR MICROCIRCUIT? OR DIE OR DICE OR LOGIC(W) CIRCUIT? OR WAFER? OR MICROELECTRONIC? OR ((CIRCUIT OR LOGIC)(2N)(CONFIGURATION))

L8 231418 S L7 AND L4

L9 7970 S L8 AND L5

L10 43 S L9 AND L1

L11 0 S L10 AND DISTAL

L12 173 S (SOLDERING OR SOLDERED OR SOLDER? OR SOLDER OR BRAZ?)(4N)(COLUMN)

L13 6 S L10 AND L3

L14 73 S L12 AND L7

L15 15 S L14 AND L5

L16 13 S L15 NOT L13

L17 147839 S (PACKAGE? OR ENCAS? OR PROTECT? OR CASING

L18 1 S L14 AND L17

L19 4 S L9 AND L2

L20 1 S L14 AND ((TIN OR SN) AND (PB OR LEAD) AND

L21 1 S L20 NOT (L13 OR L16 OR L18 OR L19)

L22 640 S L8 AND ((TIN OR SN) AND (PB OR LEAD) AND (CU OR COPPER))

L23 1 S L22 AND L12

L24 5 S L22 AND L1

L25 4 S L24 NOT (L13 OR L16 OR L18 OR L19 OR L20)

L26 30 S L8 AND L12

L27 19 S L26 NOT (L13 OR L16 OR L18 OR L19 OR L20 OR L25)

L28 184 S L8 AND L1

L29 146 S L28 NOT (L27 OR L13 OR L16 OR L18 OR L19 OR L20 OR L25)
L30 28 S L29 AND L5
L31 0 S L30 AND L3
L32 42 S (SOLDERING OR SOLDERED OR SOLDER? OR SOLDER OR BRAZ?)(4N)(COLUMNAR)
L33 16 S L32 AND L7
L34 15 S L33 NOT (L27 OR L13 OR L16 OR L18 OR L19 OR L20 OR L25)
L35 0 S L29 AND COLUMNAR(2N) INCLUSION
L36 0 S L7 AND COLUMNAR(2N) INCLUSION
L37 4 S L29 AND POLYIMIDE
L38 4 S L37 NOT (L27 OR L13 OR L16 OR L18 OR L19 OR L20 OR L25 OR L34)

L39 5 S L10 AND POLYIMIDE
L40 0 S L39 NOT (L27 OR L13 OR L16 OR L18 OR L19 OR L20 OR L25 OR L34 OR L38)
L41 348 S L9 AND (POLYIMIDE OR (POLYMERIC)(2N)(MATERIAL OR ELEMENT))
L42 36 S L14 NOT (L27 OR L13 OR L16 OR L18 OR L19 OR L20 OR L25 OR L34 OR L38 OR L39)

L43 1 S (L12 OR L32) AND DISTAL
L44 29 S (L12 OR L32) AND TERMINAL
L45 25 S L44 NOT (L27 OR L13 OR L16 OR L18 OR L19 OR L20 OR L25 OR L39 OR L38 OR L43)

L21 ANSWER 1 OF 1 WPIX (C) 2002 THOMSON DERWENT
AN 1992-032041 [04] WPIX
DNN N1992-024297
TI Low temperature controlled collapse **chip** attach process - depositing inhomogeneous anisotropic **column** of **solder** onto **solder** wettable I-O terminals without homogenising reflow.
DC U11
IN CAREY, C F; FALLON, K M; GINSBURG, R; WOYCHIK, C G
PA (IBMC) INT BUSINESS MACHINES CORP; (IBMC) IBM CORP
CYC 5
PI US 5075965 A 19911231 (199204)*
EP 485760 A1 19920520 (199221) EN 9p
R: DE FR GB
JP 04273453 A 19920929 (199245) 8p
ADT US 5075965 A US 1990-608766 19901105; EP 485760 A1 EP 1991-117796 19911018; JP 04273453 A JP 1991-281962 19911003
PRAI US 1990-608766 19901105
AB US 5075965 A UPAB: 19931006
An inhomogeneous, anisotropic **column** of **solder** is deposited from a **Pb**/**Sn** alloy onto solder wettable I/O terminals of the I/C **chip**, without subsequent homogenising reflow. The solder core has a **Pb** rich core and an **Sn** rich cap. The matching footprint of the solder wettable I/O terminals on the **microelectronic** circuit card is substantially free of deposited solder and presents a protected **Cu** surface to the **solder columns**, or, at most a surface of **Cu** and anti-oxidant.

The **chip** is aligned with the corresponding footprints on the **microelectronic** circuit card, and the solder is reflowed to bond the **chip** to the **microelectronic** circuit card.

ADVANTAGE - Joining **IC chip** to **microelectronic** circuit card

L25 ANSWER 1 OF 4 WPIX (C) 2002 THOMSON DERWENT
AN 2002-040117 [05] WPIX
DNN N2002-029646 DNC C2002-011386
TI Ball grid array interconnection structure, comprises spheres joined to module by electrically conductive adhesive comprising thermoplastic or thermosetting resin **matrix**, no-clean **solder** flux and conductive particles.
DC A85 L03 U11
IN CALL, A J; DELAURENTIS, S A; FAROOQ, S; KANG, S K; PURUSHOTHAMAN, S; STALTER, K A
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 6297559 B1 20011002 (200205)* 10p
ADT US 6297559 B1 Provisional US 1997-52175P 19970710, US 1998-107998 19980630
PRAI US 1997-52175P 19970710; US 1998-107998 19980630
AB US 6297559 B UPAB: 20020123
NOVELTY - Ball grid array structure has electrically conductive spheres joined to a **chip** carrier module by electrically conductive adhesive (ECA) and printed wiring board by solder paste respectively. ECA **contains** thermoplastic/thermosetting polymer resin **matrix**, no-clean **solder** flux and electrically conductive particles (EP) having electrically conductive fusible coating. Some EP are fused through the coating.

DETAILED DESCRIPTION - Ball gid array structure comprises an array of electrically conductive spheres (34), disposed on an electronic **chip** carrier module (31). The spheres are electrically and mechanically joined to terminal pads on the module by an electrically conductive adhesive (33). The spheres are electrically and mechanically joined to printed circuit board (36) by solder paste (35). The conductive adhesive comprises thermoplastic or thermosetting polymer resin **matrix**, no-clean **solder** flux and several electrically conductive particles. The electrically conductive particles are coated by electrically conductive and fusible coating. At least some of conductive particles are fused with each other through electrically conductive fusible coating.

USE - For interconnecting **micro-electronic packages** and printed circuit boards.

ADVANTAGE - The structure such as ball grid array **package** (BGA) has longer fatigue life. The structure provides stronger and compliant interconnections of ball grid array **package** to ceramic or plastic substrates. BGA structure is stable and does not cause an excessive inter diffusion between solder ball and adjoining solder paste.

DESCRIPTION OF DRAWING(S) - The figures show the schematic cross-sectional representation of new solder ball connection scheme in ceramic ball grid array **package**.
Module 31
Electrically conductive adhesive 33
Spheres 34
Solder paste 35
Printed circuit board 36
Dwg.3, 5/5

L25 ANSWER 2 OF 4 WPIX (C) 2002 THOMSON DERWENT
AN 2001-069604 [08] WPIX
CR 2002-120946 [67]
DNN N2001-052572 DNC C2001-019261
TI Socketable ball grid array used in pitch connections between electronic **chip** carriers and printed circuit boards has metal-coated rigid

spheres joined to the **chip** carrier terminals by electrically conducting adhesives.

DC A85 L03 P73 U11
IN CALL, A J; DELAURENTIS, S A; FAROOQ, S; KANG, S K; PURUSHOTHAMAN, S; STALTER, K A
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 6120885 A 20000919 (200108)* 7p
ADT US 6120885 A Provisional US 1997-52094P 19970710, US 1998-106779 19980630
PRAI US 1997-52094P 19970710; US 1998-106779 19980630
AB US 6120885 A UPAB: 20020308

NOVELTY - A socketable ball grid array (BGA) structure has electrically conducting and mechanically rigid spheres coated with noble contact metals joined to the **chip** carrier terminals by electrically conducting adhesives.

DETAILED DESCRIPTION - A socketable ball grid array (BGA) structure comprises electrically conducting spheres (36) that are disposed in an array on an electronic **chip** carrier (32) module. The spheres are electrically and mechanically joined to terminal pads (33) on the module by electrically conducting adhesive (34) comprising a thermoplastic or thermosetting polymer resin **matrix**, no-clean **solder** flux, and electrically conducting particles with an electrically conductive and fusible coating (35, 37). The particles are fused to the other particles through the fusible coating. An adhesive-free surface of the spheres is suitable for plug-in interconnection (38) with sockets in mating printed wiring board substrates.

USE - The socketable BGA is useful in providing pitch connections between electronic **chip** carriers or **packages** and printed circuit board. It can be used in surface mount technology (SMT).

ADVANTAGE - The invented socketable BGA is demountable and it can be plugged and unplugged to and from sockets with minimal perturbation to the ball surface facilitating component upgrade, test and burn in. The adhesive provides superior joint strengths and contact resistance values. The adhesive also provides a strong and compliant interconnection of BGA spheres to ceramic or plastic substrates, thus providing a stable joint structure that does not cause excessive interdiffusion while achieving bonding with minimal intermetallic formations.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic cross-sectional view of a new solder ball in a ceramic BGA, where the stiff and electrically conductive ball is connected to the module using an electrically conductive paste material.

Chip carrier 32
Pads 33
Electrically conducting adhesive 34
Coating 35, 37
Plug-in interconnections 38
Dwg.3/3

L25 ANSWER 3 OF 4 WPIX (C) 2002 THOMSON DERWENT
AN 1991-306534 [42] WPIX
DNN N1991-234927 DNC C1991-132812
TI **Lead** alloy solder having excellent resistance against thermal fatigue - comprises **lead** alloy matrix **contg**. **tin**, antimony and element which easily form cpd. with **tin** .
DC L03 M23 P55 U11 V04 X24
PA (TANF) TANAKA DENSHI KOGYO KK
CYC 1
PI JP 03204194 A 19910905 (199142)* 4p

JP 2807008 B2 19980930 (199844) 4p
ADT JP 03204194 A JP 1989-342784 19891229; JP 2807008 B2 JP 1989-342784 19891229
FDT JP 2807008 B2 Previous Publ. JP 03204194
PRAI JP 1989-342784 19891229
AB JP 03204194 A UPAB: 19930928
The **Pb**-alloy **solder** comprises a **Pb** alloy **matrix contg**. 1-60 wt.% **Sn**, having dispersed therein 0.01-10 wt.% of Sb and an element which easily forms a cpd. with **Sn**, so that intermetallic cpds. are dispersed in the grain boundary of SbSn cpd. crystals.

Pref. (claimed) the element which easily cpds. with **Sn** is at least one selected from **Cu**, Ni, Au, Ag, Pt, Pd, Mg, Ca, Li, In, Ce, Cd, Co, Cr, Fe, Mn, Se, Te, and Zr, which accounts for 0.01-7 wt.% of the total solder. When **Cu** or Ni is included, the upper limit of the content is each 2 wt.%, and the elements other than **Cu** and Ni are **contained** at 5 wt.% max. More pref., the **Cu** and Ni content each are 1 wt.% max.

USE/ADVANTAGE - Provides a **Pb**-alloy solder partic. useful for mounting semiconductor **chips** on substrates by flip-**chip** bonding or tape-carrier bonding.
1,6/6

L25 ANSWER 4 OF 4 JAPIO COPYRIGHT 2002 JPO
AN 1993-121869 JAPIO
TI SIMM AND ITS MANUFACTURE
IN IMAMURA KAZUYUKI; HIDA MASASHI; TANIGUCHI FUMIHIKO; YAMAGUCHI OSAMU; NAITO TOSHIHARU
PA FUJITSU LTD, JP (CO 000522)
PI JP 05121869 A 19930518 Heisei
AI JP1991-283402 (JP03283402 Heisei) 19911030
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1426, Vol. 17, No. 484, P. 151 (19930902)
AB PURPOSE: To improve connection reliability of a **solder** plated single in-**line** memory module by making a fusing point of solder plating of an outside electrode not lower than a melting heating temperature of solder cream when a **lead** of an **IC** is mounted on a component **package** electrode.
CONSTITUTION: Solder plating 5 of fusing point of 183.degree.C of 37% **lead** - 63% **tin** is applied to a thickness of 10 to 20.mu.m by electrolytic plating on a component mount electrode 3 of a 35.mu.m-thick **copper** foil printed on a printed substrate 2 of a single in-line memory module of an outside electrode and an outside electrode 4. Then, low fusing point solder cream 6 of a fusing point of 157.degree.C of 15% **lead** - 80% indium - 5% silver is applied to a thickness of 200.mu.m on the solder plating 5 alone on the component mount electrode 3. A **lead** 7 of an **IC** 1 is positioned and brought into contact with low fusing point solder cream 6 and the **IC** 1 is mounted on the printed substrate 2. Thereafter, the low fusing solder cream 6 is heated and molten at a reflow temperature of 170.degree.C and the **lead** 7 is soldered to the component mount electrode 3.

L27 ANSWER 1 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 2002-140348 [19] WPIX
DNN N2002-106187 DNC C2002-043275
TI Compliant leads has at least some of the leads arranged around neutral point of contacts, such that width dimension of some of the leads faces neutral point.
DC L03 U11
IN COICO, P A; GUERIN, L
PA (IBMC) IBM CANADA LTD
CYC 1
PI CA 2288605 A1 20010508 (200219)* EN 22p
ADT CA 2288605 A1 CA 1999-2288605 19991108
PRAI CA 1999-2288605 19991108
AB CA 2288605 A UPAB: 20020321
NOVELTY - Each lead extends outwardly from a respective contact on the surface of the **IC package** (30), and has a width dimension that is greater than the thickness dimension. At least some of the leads are arranged around a neutral point of the contacts, so that the width dimension of some of the leads faces the neutral point.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for an electronic circuit assembly.

USE - For interconnecting area array surface mounted components to printed circuit boards.

ADVANTAGE - Provides increased reliability in interconnections in the presence of thermal stress. Provides new, practical and more reliable compliant interconnection element for interconnecting electronic circuit components. Aligns flat connection elements in the orientation of optimal compliance and flexibility, thereby offering compliance to thermal variation that is superior to that of commonly used **solder** balls or **columns**. Provides interconnections from one planar substrate to another.

DESCRIPTION OF DRAWING(S) - The figure is the side cross-sectional view of an **IC package** assembled on a printed circuit card.

IC Package 30

Dwg.6/7

L27 ANSWER 2 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 2001-662084 [76] WPIX
CR 2000-363798 [29]
DNN N2001-493191
TI Stacked semiconductor device manufacturing method for implantable medical equipment, involves stacking semiconductor **dies** attached to tapes in vertical direction during columnar solder connections.
DC S05 U11
IN HUBBARD, R L
PA (MEDT) MEDTRONIC INC
CYC 1
PI US 6168973 B1 20010102 (200176)* 25p
ADT US 6168973 B1 Div ex US 1998-143141 19980828, US 1999-292423 19990415
FDT US 6168973 B1 Div ex US 6051887
PRAI US 1998-143141 19980828; US 1999-292423 19990415
AB US 6168973 B UPAB: 20011227
NOVELTY - The semiconductor **dies** (52,62) attached to respective single and double metal layered tapes (54,64) are stacked in vertical direction using columnar solder connections (46). The solder connections are formed from solder balls attached to pad regions on the sides of tapes.

USE - For manufacturing stacked semiconductor device used in dual line packaging and **chip** scale **package** of memory device used in implantable medical equipment such as pacemaker-cardioverter defibrillator.

ADVANTAGE - Improves mounting density of **die** on circuit board, thus simultaneously enhancing mass producibility of stacked semiconductor **die** in cost effective manner.

DESCRIPTION OF DRAWING(S) - The figure shows the exploded end view of stacked semiconductor device.

Solder connections 46

Semiconductor **dies** 52,62

Tapes 54,64

Dwg.4/14

L27 ANSWER 3 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 2001-353676 [37] WPIX
DNN N2001-256823 DNC C2001-109525
TI Ceramic substrate for **integrated circuit packages**, includes ceramic material having coefficient of expansion that matches that of printed circuit board material.
DC L03 P73 U11
IN VODRAHALLI, N K
PA (HICK-I) HICKMAN P L
CYC 1
PI US 6228468 B1 20010508 (200137)* 8p
ADT US 6228468 B1 Provisional US 1996-21006P 19960726, US 1997-901024 19970725
PRAI US 1996-21006P 19960726; US 1997-901024 19970725
AB US 6228468 B UPAB: 20010704

NOVELTY - Ceramic substrate includes ceramic material having a coefficient of expansion that matches that of printed circuit board material.

DETAILED DESCRIPTION - A ceramic substrate (48) includes two layers of ceramic material. Each layer is formed comprises a mixture of 50-99 wt.% magnesium oxide and glass and has a coefficient of expansion between 5-16 PPM/ deg. C.

USE - The substrate is used for **integrated circuit packages** such as ball grid array **packages**.

ADVANTAGE - The invention gives the ability to use high density aspects of multilayer ceramic substrates and allows the use of existing infrastructure for manufacturing multilayer ceramic without changing production costs. It permits the use of solder ball interconnects, which are robust and are without the handling issues the pinned and **solder column packages** have. The **solder** ball interconnection also allows easy testing of the **packages**. It provides for robustness and reliability of the connection between the **package** and the printed circuit board. It thus provides for an overall system reliability.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of a ceramic **package**.

Ceramic substrate 48

Dwg.2/3

L27 ANSWER 4 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 2000-636834 [61] WPIX
DNN N2000-472136
TI **Encapsulated** tapeless board-on-**chip** (BOC) with exposed backside silicon **chip**.
DC U11 U14
IN ENG, K T; YEW, C K
PA (TEXI) TEXAS INSTR SINGAPORE PTE LTD

CYC 1
PI SG 74060 A1 20000718 (200061)*
ADT SG 74060 A1 SG 1998-1733 19980707
PRAI SG 1998-1733 19980707
AB SG 74060 A UPAB: 20001128
NOVELTY - The present invention includes a method and apparatus for exposing one side of a semiconductor **chip** by forming an adhesive on a PCB substrate. The adhesive layer is attached between the semiconductor **chip** and the PCB substrate. **Solder columns** are formed to connect the semiconductor **chip** with an external device.
USE - None given.
Dwg.0/0

L27 ANSWER 5 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 2000-577145 [54] WPIX
DNN N2002-118071 DNC C2002-048624
TI **Chip** assembly for electronic components or modules, includes silicone adhesive between semiconductor **chip** and cap.
DC A85 L03 P73 U11
IN CARON, A A; COFFIN, J T; POMPEO, F L; ZITZ, J A
PA (IBMC) INT BUSINESS MACHINES CORP; (CARO-I) CARON A A; (COFF-I) COFFIN J T; (POMP-I) POMPEO F L; (ZITZ-I) ZITZ J A
CYC 2
PI KR 99023641 A 19990325 (200054)*
US 2001040006 A1 20011115 (200221)B 11p
ADT KR 99023641 A KR 1998-33254 19980817; US 2001040006 A1 Div ex US 1997-918615 19970822, US 1999-241238 19990201
PRAI US 1997-918615 19970822; US 1999-241238 19990201
AB US2001040006 A UPAB: 20020403 ABEQ treated as Basic
NOVELTY - A **chip** assembly comprises a substrate, semiconductor **chip**(s) mounted on upper surface of the substrate, a cap covering the **chip** and the upper surface, a silicone adhesive between the **chip** and cap.
DETAILED DESCRIPTION - A **chip** assembly comprises a substrate (12), semiconductor **chip**(s) (14) mounted on upper surface of the substrate, a cap (11) covering the **chip** and the upper surface, a silicone adhesive (25) between the **chip** and cap. The adhesive has sufficient bond strength to secure the cap to the **chip** without additional mechanical constraint while providing a direct thermally conductive path and permitting heat flow from the **chip** to the cap to maintain steady state operation of the semiconductor **chip**.
An INDEPENDENT CLAIM is also included for a method of providing a direct thermally conductive path between at least one **chip** and at least one heatsink cap, by applying a silicone adhesive between a semiconductor **chip** and cap, securing the cap to a substrate by a mechanical fixture, curing the silicone substrate, and removing the mechanical fixture.
USE - As a **chip** assembly for electronic components or modules.
ADVANTAGE - The invention has a thermally conductive mechanically robust path between at least one **chip** and at least one cooling member. It increases the available area on the substrate or **chip** carrier for joining active devices such as **chips** or passive devices such as capacitors and resistors. It minimizes thermal performance degradation over the **chip** carrier life, and absorbs thermally inducted strain without damage to the **chip** carrier or associated devices. It ensures the mechanical and operational integrity of the bond

between devices and the cooling member under typical use conditions such as gravity, mechanical shock, vibration, high temperature with humidity and repeated thermal expansion/contraction cycles due to temperature variation.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional elevational view of the invention.

Cap 11

Substrate 12

Semiconductor **chip**(s) 14

Solder balls 15

Underfill material 18

Silicone adhesive 25

Dwg.2/8

AB KR 99023641 A UPAB: 20020409

NOVELTY - A **chip** assembly comprises a substrate, semiconductor **chip**(s) mounted on upper surface of the substrate, a cap covering the **chip** and the upper surface, a silicone adhesive between the **chip** and cap.

DETAILED DESCRIPTION - A **chip** assembly comprises a substrate (12), semiconductor **chip**(s) (14) mounted on upper surface of the substrate, a cap (11) covering the **chip** and the upper surface, a silicone adhesive (25) between the **chip** and cap. The adhesive has sufficient bond strength to secure the cap to the **chip** without additional mechanical constraint while providing a direct thermally conductive path and permitting heat flow from the **chip** to the cap to maintain steady state operation of the semiconductor **chip**.

An INDEPENDENT CLAIM is also included for a method of providing a direct thermally conductive path between at least one **chip** and at least one heatsink cap, by applying a silicone adhesive between a semiconductor **chip** and cap, securing the cap to a substrate by a mechanical fixture, curing the silicone substrate, and removing the mechanical fixture.

USE - As a **chip** assembly for electronic components or modules.

ADVANTAGE - The invention has a thermally conductive mechanically robust path between at least one **chip** and at least one cooling member. It increases the available area on the substrate or **chip** carrier for joining active devices such as **chips** or passive devices such as capacitors and resistors. It minimizes thermal performance degradation over the **chip** carrier life, and absorbs thermally inducted strain without damage to the **chip** carrier or associated devices. It ensures the mechanical and operational integrity of the bond between devices and the cooling member under typical use conditions such as gravity, mechanical shock, vibration, high temperature with humidity and repeated thermal expansion/contraction cycles due to temperature variation.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional elevational view of the invention.

Cap 11

Substrate 12

Semiconductor **chip**(s) 14

Solder balls 15

Underfill material 18

Silicone adhesive 25

Dwg.2/8

L27 ANSWER 6 OF 19 WPIX (C) 2002 THOMSON DERWENT

AN 2000-022143 [02] WPIX

DNN N2000-016393
TI Electrical contract for test board used in testing **IC package**.
DC S01 U11 V04
IN BUSCHBOM, M L
PA (TEXI) TEXAS INSTR INC
CYC 1
PI US 5982186 A 19991109 (200002)* 5p
ADT US 5982186 A US 1996-719530 19960927
PRAI US 1996-719530 19960927
AB US 5982186 A UPAB: 20000112
NOVELTY - The contacts (16) are formed on the surface of the membrane carrier (12), by diamond particle, carbides and oxides. The contacts are connected to the terminals (18) that are used as plated through-holes. The pins (14) supported by a plastic frame (20) are connected to the terminals.

DETAILED DESCRIPTION - The resilient pad (24) is arranged between the carrier and the PCB. The pins are inserted in the through holes (26) in the PCB.

USE - For test board used in testing **IC package** e.g. BGA **package**. Other surface mount technologies include SGA **package**, **solder column** array, land grid array, quad flat pack, flat pack, plastic leaded **chip** carrier, SOIC, pin grid **package**, SIM module, 3D stack, shrink small outline **package**.

ADVANTAGE - Avoids need for soldering of contact with PCB by inserting directly into through hole. Reduces time required to install/remove carrier from tester board. Avoids damage of electronic circuit on PCB by heat by avoiding installation/removal of contactor by soldering. Reduces number of spare tester boards. Facilitates quick replacement of contactor.

DESCRIPTION OF DRAWING(S) - The figure shows connecting process of **IC** to test board using contactor.
Contactor 10
Membrane carrier 12
Pin 14
Contact 16
Terminal 18
Frame 20
Resilient pad 24
Through hole 26
Dwg.2/3

L27 ANSWER 7 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 1999-570670 [48] WPIX
DNN N1999-420387 DNC C1999-166526
TI Dual surface seal for **encapsulating** ceramic semiconductor **chip** carriers.
DC A21 A31 A85 L03 U11
IN POMPEO, F L; TOY, H T
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 5956576 A 19990921 (199948)* 9p
ADT US 5956576 A US 1996-713378 19960913
PRAI US 1996-713378 19960913
AB US 5956576 A UPAB: 19991122
NOVELTY - A cover (20) is mated to a substrate (10) by applying a material layer (50) to horizontal and vertical surfaces of substrate edges and placing a peripheral edge of the cover over at least a portion of the

layer to secure at least part of the horizontal and vertical surfaces of the cover edge.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following: (a) an electronic device comprising a substrate and cover secured to one another by a seal band as above; and (b) an electronic device comprising cover, substrate and lid in which substrate and cover and lid and cover are mutually secured as above.

USE - In providing a fluid-tight seal to a ceramic **chip** carrier using dual surfaces (claimed) for high-density electronic devices

ADVANTAGE - The top surface area required for sealing is minimized so that components can be more efficiently **packaged**: the seal can be hermetic or non-hermetic.

DESCRIPTION OF DRAWING(S) - A cross-section of the carrier assembly is shown.

Substrate 10
Chip 16
Cover 20
Seal 50
Dwg.3/7

L27 ANSWER 8 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 1998-011357 [02] WPIX
DNN N1998-008968
TI **Microelectronic package** for **integrated circuit chip** - has two substrates adjacent one another with arched **solder columns** extending from one substrate to other forming quarter or half rings depending on orientation of substrates.
DC T04 U11 U14
IN DEANE, P A; RINNE, G A
PA (MCNC-N) MCNC
CYC 22
PI EP 810661 A2 19971203 (199802)* EN 17p
R: AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
JP 10163413 A 19980619 (199835) 46p
US 5793116 A 19980811 (199839)
KR 97078788 A 19971212 (199850)
US 5963793 A 19991005 (199948)
TW 440982 A 20010616 (200203)
KR 286056 B 20010416 (200218)
ADT EP 810661 A2 EP 1997-303591 19970527; JP 10163413 A JP 1997-138944 19970528; US 5793116 A US 1996-654539 19960529; KR 97078788 A KR 1997-21710 19970529; US 5963793 A Div ex US 1996-654539 19960529, US 1998-96754 19980612; TW 440982 A TW 1997-107544 19970602; KR 286056 B KR 1997-21710 19970529
FDT US 5963793 A Div ex US 5793116; KR 286056 B Previous Publ. KR 97078788
PRAI US 1996-654539 19960529; US 1998-96754 19980612
AB EP 810661 A UPAB: 19980112
The **microelectronic package** includes a first **microelectronic** substrate (100). A second **microelectronic** substrate (200) is positioned so that an edge (200a) of the second substrate is adjacent the first substrate. Several arched **solder columns** (320) extend from next to the edge of the second substrate to the first substrate.

The second substrate is not parallel to the first, and is preferably orthogonal to it. The arched **solder columns** form several quarter rings which extend from next to the edge of the second substrate to the first substrate. The second substrate can be coplanar with the first with the edge of each being adjacent. The **solder**

columns form half rings from next to the edge of the first to the second substrates.
USE - For connecting several **integrated circuit dies** in **package**.
ADVANTAGE - Simplifies connection of several **dice** due to solder bump expansion.
Dwg.3b/12

L27 ANSWER 9 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 1997-112461 [11] WPIX
DNN N1997-093031
TI Reflow solder processing method for installation of MCM substrate on large scale substrate - involves arranging **solder column** between MCM substrate and large scale substrate, that carries out inner **package** of column like copper cylinder on pad, which has solder material on outer surface.
DC U11 U14 V04 X24
PA (NIDE) NEC SHIZUOKA LTD
CYC 1
PI JP 08316629 A 19961129 (199711)* 4p
ADT JP 08316629 A JP 1995-116889 19950516
PRAI JP 1995-116889 19950516
AB JP 08316629 A UPAB: 19970313
The method involves high density installation of circuit components such as **IC**, LSI **chip**, a resistor and a capacitor on an MCM substrate. The MCM substrate is then installed on a large scale substrate using a **solder column** (16). The **solder column** carries out inner **package** of a column shaped copper cylinder (19) on a pad and has a solder material (18) in outer surface. The **solder column** is installed between the MCM substrate and large scale substrate, and is heated by a reflow heat treatment.
The **solder** material of **solder column** dissolves and an alloy connection of both substrates is carried out when heat treated. The copper cylinder serves as spacer that keeps a constant gap between the substrates.
ADVANTAGE - Secures stable high density installation of substrate even with narrow pad space. Improves versatility of component installation.
Dwg.1/2

L27 ANSWER 10 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 1996-454490 [45] WPIX
CR 1993-095268 [12]; 1996-229907 [23]
DNC C1996-142380
TI Cleavable di epoxide compsns. for **encapsulation** of electronic devices - **contg**. di epoxide having cleavable acyclic acetal gp., cyclic di carboxylic anhydride curing agent, 1,3-diaza catalyst, etc..
DC A21 A85 A96 A97 B07 C07 E19 L03
IN AFZALI-ARDAKANI, A; BUCHWALTER, S L; GELORME, J D; KOSBAR, L L; NEWMAN, B H; POMPEO, F L
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 5560934 A 19961001 (199645)* 14p
ADT US 5560934 A CIP of US 1991-755253 19910905, Div ex US 1994-210879 19940318, US 1995-480403 19950607
FDT US 5560934 A Div ex US 5512613
PRAI US 1994-210879 19940318; US 1991-755253 19910905; US 1995-480403

19950607
AB US 5560934 A UPAB: 19961111
Diepoxide compsns. (I) for **encapsulation** and **protection** of electronic devices and assemblies, comprises the cured reaction prod. of: (a) a diepoxide **contg**. a cleavable acyclic acetal gp. between the 2 epoxy gps.; (b) a cyclic dicarboxylic anhydride curing agent; (c) a 1,3-diaza catalyst cpd. having 2 nitrogen atoms with 1 nitrogen doubly bonded to a central carbon and singly bonded to 1 other carbon, and the other nitrogen singly bonded to the central carbon and singly bonded to 2 other carbons; opt. (d) a tert. amine catalyst; and (e) a hydroxy functional initiator.

(I) is capable of being readily cleaved and removed in acidic organic solvents.

(I) additionally **contains** a flexibiliser comprising butadiene-acrylonitrile rubber, polyethylene glycol, polypropylene glycol poly(caprolactone)diol, poly(oxybutylene)diol or poly(butadiene)/maleic anhydride adducts.

USE - The electronic device is a silicon **integrated circuit** electrically connected to a substrate with solder using controlled collapse **chip** connection, **solder** balls or **columns**, flip **chip** attachment, or wire bonding. The substrate is a ceramic multi-**chip** module or printed circuit card. The device comprises an assembly of a silicon device directly attached to a printed circuit card, or semiconductor **chips** **encapsulated** in moulded plastic which are surface mounted with reinforced solder joints to a printed circuit card. The compsns. are applied as a globtop encapsulant. (all claimed). Slow degrading compsns. can also be used for **encapsulation** of fertilisers, pharmaceuticals or pesticides (claimed) for biodegradable consumer packaging.

ADVANTAGE - The **encapsulating** compsns. can be degraded by application of solvent systems to allow maintenance, e.g. for repair, replacement, recovery or recycling of parts. Removal of the epoxy allows replacement of obsolete or defective devices, saving the cost of discarding other valuable components in a **microelectronic** assembly.

Dwg.0/5

L27 ANSWER 11 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 1993-320004 [40] WPIX
DNN N1993-246577 DNC C1993-142375
TI Solder finishing system for planar leaded flat **package** **integrated circuits** - utilises gravity to minimise splatter, splashing and bridging.
DC L03 M23 U11 V04
IN DOHERTY, R H; WOOD, R C
PA (NASC) NAT SEMICONDUCTOR CORP
CYC 2
PI US 5248520 A 19930928 (199340)*
CA 2089434 A 19930814 (199344)
ADT US 5248520 A US 1992-835208 19920213; CA 2089434 A CA 1993-2089434 19930212
PRAI US 1992-835208 19920213
AB US 5248520 A UPAB: 19931129
An automated method for finishing the leads of an **integrated circuit** (**IC**) flat **package** having first and second rows of leads coplanar with the flat **package** along respective first and second sides of the flat **package**, comprises a) establishing a vertical first falling **column** of falling

molten **solder**; b) orientating the flat **package** at a first downwardly depending angle intermediate between horizontal and vertical orientations with the first side on the lower side of the flat **package** and with the first row of leads depending downward from the lower side at said fist downwardly depending angle; c) conveying the flat **package** at the first downwardly depending angle adjacent to the first falling **column** of molten **solder** and immersing the first row of leads in the falling column at said downwardly depending angle to enhance runoff and reduce spatter and bridging; d) establishing a vertical second falling **column** of falling molten **solder**; e) automatically reorienting the flat **package** at a second downwardly depending angle opposite the first downwardly depending angle and intermediate between horizontal and vertical orientations with the second side on the lower side of the flat **package** and with the second row of leads depending downward from the power side at salid second downwardly depending angle; and f) conveying the flat **package** at the second downwardly depending angle adjacent to the second falling **column** of molten **solder** and immersing the second row of lead in the second falling column at the second downwardly depending angle to enhance runoff and reduce spatter and bridging. The step of reorienting the flat **package** to the opposite second downwardly depending angle comprises lifting the flat **package** at the first downwardly depending angle, swinging the flat **package** through an arc, and depositing the flat **package** at the second downwardly depending angle.

L27 ANSWER 12 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 1989-370879 [50] WPIX
DNN N1989-282288 DNC C1989-164248
TI High voltage breakdown semiconductor diode(s) - mfd. without high-accuracy alignment steps.
DC L03 U11 U12
IN DENNER, V; HERDEN, W
PA (BOSC) BOSCH GMBH ROBERT
CYC 12
PI WO 8911734 A 19891130 (198950)* EN 8p
RW: AT BE CH DE FR GB IT LU NL SE
W: JP US
ADT WO 8911734 A WO 1988-EP456 19880521
PRAI WO 1988-EP456 19880521
AB WO 8911734 A UPAB: 19930923
High voltage breakdown diodes of the type comprising a number of individual p-n junction diodes electrically connected in series are mfd. by first cutting a **wafer** having layers of p-type material (11,13) and n-type material (12,14) to form individual diodes and then profiling the external surfaces of each diode at the p-n junction so that it is no perpendicular to the plane (B) of the p-n junction. The profilling step is carried out by trench etching or by using a suitably profiled grinding wheel after the diodes have been **soldered** together to form a **column**. Pref. the diodes are **encased** together ina glass after the profiling step.
USE/ADVANTAGE - The method is simpler to carry out than known methods since there are no glass passivations to be aligned when the individual diodes are formed into columns and the method does not involve cutting through glass passivations.
6/6

L27 ANSWER 13 OF 19 WPIX (C) 2002 THOMSON DERWENT

AN 1989-221740 [31] WPIX
DNN N1989-169201 DNC C1989-098452
TI Heat treating low m.pt. metal esp. a **chip solder** coating - using **column** of heated oil with a controlled temp. gradient.
DC L03 M22 M23 P53 U11 V01 V04
IN HIRAOKA, I; HIRAYAMA, H; SAITO, I; SHINDO, Y; TSUJIMOTO, Y
PA (MATU) MATSUSHITA ELEC IND CO LTD; (SUMM) SUMITOMO METAL MINING CO
CYC 4
PI EP 325660 A 19890802 (198931)* EN 12p
R: DE FR GB
US 4842654 A 19890627 (198933) 9p
EP 325660 B1 19920923 (199239) EN 12p
R: DE FR GB
DE 3874878 G 19921029 (199245)
ADT EP 325660 A EP 1988-100804 19880120; US 4842654 A US 1988-145403 19880119; EP 325660 B1 EP 1988-100804 19880120; DE 3874878 G DE 1988-3874878 19880120, EP 1988-100804 19880120
FDT DE 3874878 G Based on EP 325660
PRAI EP 1988-100804 19880120
AB EP 325660 A UPAB: 19930923
Low m.pt. metal is heat-treated by: placing a high b.pt. liq., e.g. oil, in a tubular **container** with a heater at an upper portion to establish a temp. gradient ranging from a high temp. above the metal m.pt. to a low temp. below its m.pt.; and allowing the metal to move from the high temp. zone to the low temp. zone so that metal on the surface is first melted and then solidified.
USE - Esp. in treating the solder-coated electrodes of **chip** parts (claimed) e.g. resistors, in miniaturised devices etc. to ensure soldering reliability.
4/6

L27 ANSWER 14 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 1988-001721 [01] WPIX
DNN N1988-001358 DNC C1988-000786
TI Solder finishing **IC package** leads - by conveying through vertical **columns** of **solder**, and using hot gas jets to remove surplus solder.
DC L03 M23 P42 P55 U11 X24
IN WOOD, R C
PA (FAIH) FAIRCHILD SEMICONDUCTOR CORP
CYC 9
PI EP 251879 A 19880107 (198801)* EN 10p
R: DE FR GB IT NL
US 4720396 A 19880119 (198805) 10p
JP 63072478 A 19880402 (198819)
CA 1247753 A 19881228 (198905)
EP 251879 B1 19920812 (199233) EN 11p
R: DE FR GB IT NL
DE 3781050 G 19920917 (199239)
JP 07008431 B2 19950201 (199509)
KR 9513051 B1 19951024 (199901)
ADT EP 251879 A EP 1987-401417 19870623; US 4720396 A US 1986-878307 19860625; JP 63072478 A JP 1987-156702 19870625; EP 251879 B1 EP 1987-401417 19870623; DE 3781050 G DE 1987-3781050 19870623, EP 1987-401417 19870623; JP 07008431 B2 JP 1987-156702 19870625; KR 9513051 B1 KR 1987-6405 19870624
FDT DE 3781050 G Based on EP 251879; JP 07008431 B2 Based on JP 63072478
PRAI US 1986-878307 19860625

AB EP 251879 A UPAB: 19930923
The leads of an **integrated circuit package** having parallel rows of leads along each side are solder finished at the ends by conveying the **package** between two vertical **columns** of molten **solder** such that the leads only are immersed in the columns, and directing hot nitrogen gas onto the soldered leads to simultaneously dry the deposited coating, whilst removing the excess solder.

Appts. comprises, an **IC** conveyor having a lead soldering station comprising a pair of molten solder delivery pipes, positioned to discharge solder streams either side of the conveyed I.C **package** , hot gas outlet pipes, solder collecting and pumping equipment.

USE/ADVANTAGE - The method is useful for solder finishing the leads of I.C. **packages**, the application of the **solder** by vertical **columns** prevents bridging of the **solder** and accumulation of excessive coating. Additionally, the conveyor track system may be integrated with conventional chain conveyors and provides a new solder bridge track section which allows immersion of the leads whilst preventing contact and immersing of the conveyor carriers with the solder.
1/6

L27 ANSWER 15 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 1987-023935 [04] WPIX
DNN N1987-018100 DNC C1987-009898
TI Electronic component connection device - has conductive joint forming members mounted in apertures in retaining member.
DC L03 M23 P55 U11 U14 V04
IN ALLEN, L J; CHERIAN, G; DIAZ, S H
PA (RAYC) RAYCHEM CORP
CYC 1
PI GB 2177643 A 19870128 (198704)*
GB 2177643 B 19880203 (198805)
ADT GB 2177643 A GB 1984-18887 19840702; GB 2177643 B GB 1986-18887 19850713
PRAI US 1983-509684 19830630; US 1984-610077 19840514
AB GB 2177643 A UPAB: 19930922
Retaining member (22) has a number of apertures (26) spaced to correspond to pre-selected points on an electrically conductive element each aperture **containing** and supporting a preform (28) of electrically conductive joint forming material with the ends of the preforms arranged to contact the preselected points on the element. The joint forming material is filled solder, supported solder, or conductive elastomer which retains its preform shape while the solder is molten or the elastomer softens.

Solder column for forming electrical connections is also claimed. The solder **contains** particles or filaments which are solid at a temp. at which the solder is molten and which maintain the solumn like shape when the solder is molten.

USE/ADVANTAGE - Appts. is for attaching electronic components, especially **chips** or **chip** carrier **packages** to each other or to supporting substrates such as circuit boards. Appts. provides connection forming material in a predetermined shape which is retained during formation of the joint and provides a reliable resilient connection which is able to withstand fatigue and repetitive thermal cycling, and will accommodate dimensional irregularities in the components.
4/11

L27 ANSWER 16 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 1987-023934 [04] WPIX

DNN N1987-018099 DNC C1987-009897
TI Electronic component carrier device - with conductive joint forming members mounted in apertures in retaining member.
DC L03 M23 P55 U11 U14 V04
IN ALLEN, L J; CHERIAN, G; DIAZ, S H
PA (RAYC) RAYCHEM CORP
CYC 1
PI GB 2177642 A 19870128 (198704)*
GB 2177642 B 19880203 (198805)
ADT GB 2177642 A GB 1984-18886 19840702; GB 2177642 B GB 1986-18886 19850713
PRAI US 1983-509684 19830630; US 1984-610077 19840514
AB GB 2177642 A UPAB: 19930922
Retaining member (22) has a number of apertures (26) spaced to correspond to pre-selected points on an electrically conductive element each aperture **containing** and supporting a preform (28) of electrically conductive joint forming material with the ends of the preforms arranged to contact the preselected points on the element. The joint forming material is filled solder, supported solder, or conductive elastomer which retains its preform shape while the solder is molten or the elastomer softens.

Also claimed is a **solder column** for forming electrical connections, the solder **containing** particles or filaments which are solid at a temperature at which the solder is molten and which maintain the **column** like shape when the **solder** is molten.

USE/ADVANTAGE - Attaching electronic components, especially **chips** or **chip** carrier **packages** to each other or to supporting substrates such as circuit boards. Provides connection forming material in a predetermined shape which is retained during formation of the joint and provides a reliable resilient connection which is able to withstand fatigue and repetitive thermal cycling, and will accommodate dimensional irregularities in the components.
4/14

L27 ANSWER 17 OF 19 JAPIO COPYRIGHT 2002 JPO
AN 2000-156461 JAPIO
TI HIGH-INTEGRATION **CHIP**-ON-**CHIP** PACKAGING
IN BERTIN CLAUDE L; FERENCE THOMAS GEORGE; WAYNE JOHN HOWEL; SPROGIS EDMUND J
PA INTERNATL BUSINESS MACH CORP <IBM>
PI JP 2000156461 A 20000606 Heisei
AI JP1999-151409 (JP11151409 Heisei) 19990531
PRAI US 1998-105419 19980626
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To individually set a **chip** and to achieve a compact semiconductor **package** with a high-integration technique by equipping a plurality of independent **chips** that are electrically connected and function completely and **chip**-on-**chip** part connection/interconnection for electrically connecting the **chips** to an external circuit.
SOLUTION: **Chip**-on-**chip** parts 10 include a first **chip** 30, a second **chip** 40, and **chip**-on-**chip** part connection 20. An active region 35 of the first **chip** 30 is electrically connected to an active region 45 of the second **chip** 40 via solder ball connection 50 or electrical connection between **chips**. Also, the **chip**- on-**chip** part connection 20 is a **solder column** 22 that is connected to the first **chip** 30, and the **solder column** 22 can connect the **chip**-on-**chip** parts 10 to an external circuit via a substrate, thus achieving a reliable,

compact semiconductor **package** with high-integration technique and at the same time improving thermal performance.

L27 ANSWER 18 OF 19 JAPIO COPYRIGHT 2002 JPO
AN 1999-297889 JAPIO
TI SEMICONDUCTOR **PACKAGE**, MOUNTING BOARD AND MOUNTING METHOD BY USE OF THEM
IN OYA YOICHI
PA SONY CORP
PI JP 11297889 A 19991029 Heisei
AI JP1998-106424 (JP10106424 Heisei) 19980416
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 99
AB PROBLEM TO BE SOLVED: To ensure a semiconductor **package** of joint strength by a conductive material layer to enhance it in mounting reliability even if terminals provided onto a relay board corresponding to the input/output terminals of a semiconductor **chip** are micronized and lessened in pitch.
SOLUTION: The **package** side lands 3a of a semiconductor **package** P1 are fully exposed inside an opening 5a provided in a solder resist layer 5. The board side land 12a of a mounting board B1 are fully exposed inside an opening 13a provided in a solder resist layer 13. When the semiconductor **package** P1 and the mounting board B1 are joined together through the intermediary of a solder layer 14a, the solder layer 14a is brought into contact with the lands 3a and 12a by creeping over their side walls, so that a joint between the **package** P1 and the mounting board B1 is enhanced in joint strength due to an increase in contacting area and a shape effect. When the lands 3a and 12a are set equal to each other in dimension and shape, the **solder** layer 14a becomes a **column** uniform in sectional area, so that stress is prevented from concentrating locally on the solder layer 14a.

L27 ANSWER 19 OF 19 JAPIO COPYRIGHT 2002 JPO
AN 1997-017795 JAPIO
TI BUMP STRUCTURE
IN MATSUSHITA HIKARI
PA NEW JAPAN RADIO CO LTD, JP (CO 326320)
PI JP 09017795 A 19970117 Heisei
AI JP1995-187887 (JP07187887 Heisei) 19950630
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 97, No. 1
AB PURPOSE: To provide a solder bump structure which can be **protected** against cracking, restrained from being separated from a board electrode due to a thermal stress applied after a flip **chip** is mounted, and manufactured at a low cost.
CONSTITUTION: A bump structure is formed on the electrode of a flip **chip** semiconductor device, wherein the bump structure is composed of a barrier metal 2 laminated on an electrode pad 1 of a semiconductor device, metal columns 3 provided upright on the barrier metal 2, a core bump 4 laminated spreading over the metal **columns** 3, and a **solder** bump 5 laminated on the core bump 4.

L34 ANSWER 1 OF 15 WPIX (C) 2002 THOMSON DERWENT
AN 2000-484738 [43] WPIX
DNN N2000-360403 DNC C2000-145981
TI Semiconductor **wafer** for **chip** sized semiconductor devices has columnar electrodes with plated tops for bonding to external terminals.
DC L03 U11
IN IHARA, Y; KOBAYASHI, T; WAKABAYASHI, S
PA (SHIA) SHINKO ELECTRIC IND CO LTD
CYC 28
PI EP 1024531 A2 20000802 (200043)* EN 22p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
JP 2000216111 A 20000804 (200051) 7p
JP 2000216185 A 20000804 (200051) 9p
KR 2000053618 A 20000825 (200121)
TW 444288 A 20010701 (200220)
ADT EP 1024531 A2 EP 2000-300613 20000127; JP 2000216111 A JP 1999-18229 19990127; JP 2000216185 A JP 1999-18237 19990127; KR 2000053618 A KR 2000-3629 20000126; TW 444288 A TW 2000-101296 20000126
PRAI JP 1999-18237 19990127; JP 1999-18229 19990127
AB EP 1024531 A UPAB: 20000907
NOVELTY - A semiconductor **wafer** has columnar electrodes (24) connected to wiring lines and with plated tops (41) for bonding to external terminals. The **wafer** is encapsulated except for the tops of the columnar electrodes.
DETAILED DESCRIPTION - A semiconductor **wafer** comprises columnar electrodes (24) and electrode terminals on its surface, an insulation film on which patterned wiring lines (27) are formed which are connected to an electrode terminal at one end and to a columnar electrode at the other and an encapsulating layer from which the top of the columnar electrodes are exposed. These electrodes are provided with nickel/nickel alloy (Ni/Ni alloy), palladium and gold films successively plated at their tops (41).
INDEPENDENT CLAIMS are also included for methods of producing the **wafer** above and for a semiconductor device comprising the **wafer** above.
USE - Semiconductor **wafers** for **chip**-sized packages.
ADVANTAGE - The **columnar** electrodes have increased **solder** wettability, giving firmer bonding to an external terminal such as a solder ball and device reliability is increased.
DESCRIPTION OF DRAWING(S) - A section of the semiconductor **wafer** is shown.
Columnar electrodes 24
Wiring lines 27
Plated films 41
Dwg.3D/12

L34 ANSWER 2 OF 15 WPIX (C) 2002 THOMSON DERWENT
AN 2000-363798 [31] WPIX
CR 2001-662084 [12]
DNN N2000-272144
TI Semiconductor stacked memory device for implantable medical apparatus, includes substrate source whose conductive traces are connected by solder balls, with semiconductor **die** between the substrates.
DC U11
IN HUBBARD, R L

PA (MEDT) MEDTRONIC INC
CYC 1
PI US 6051887 A 20000418 (200031)* 22p
ADT US 6051887 A US 1998-143141 19980828
PRAI US 1998-143141 19980828
AB US 6051887 A UPAB: 20011227
NOVELTY - The substrates (54,64) with semiconductor **dies** (52,62) include conductive traces for connecting with **die** bond pads. **Columnar solder** ball connections formed by solder balls attached to the substrates connect the conductive traces of the substrates such that **die** (62) is configured between substrates.
DETAILED DESCRIPTION - The conductive traces of one of the substrate (64) connect the two substrates together, while those on the other side connect with **die** bond pads.
USE - For use in implantable medical devices such as pacemakers, in portable electronic devices.
ADVANTAGE - Low profile can be achieved and the device can be easily mounted to PCB. Is mass producible, cost effective. Has compatible interconnection density. The total thickness of the device is 60-70 mil, thus reducing space consumption.
DESCRIPTION OF DRAWING(S) - The figure shows perspective view of semiconductor stacked device.
Semiconductor **dies** 52,62
Substrates 54,64
Dwg.3/14

L34 ANSWER 3 OF 15 WPIX (C) 2002 THOMSON DERWENT
AN 1988-223253 [32] WPIX
TI Lead pin for **IC** electrode - has regular tetrahedral, cube, globular or **columnar soldering** silver paste deposited on head NoAbstract Dwg 0/12.
DC U11
PA (MITA) MITSUI & CO LTD; (TOJH) TOKURIKI HONTEN KK
CYC 1
PI JP 63157454 A 19880630 (198832)* 7p
ADT JP 63157454 A JP 1986-306088 19861222
PRAI JP 1986-306088 19861222

L34 ANSWER 4 OF 15 JAPIO COPYRIGHT 2002 JPO
AN 2001-284381 JAPIO
TI SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE
IN TAKAO YUKIHIRO
PA SANYO ELECTRIC CO LTD
PI JP 2001284381 A 20011012 Heisei
AI JP2000-092688 (JP2000092688 Heisei) 20000330
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2001
AB PROBLEM TO BE SOLVED: To enhance reliability at mounting of a **chip** size package.
SOLUTION: A columnar terminal 9 having constricted side face, where the area of upper surface is larger than the area of bottom face, is formed and a solder ball 12 is mounted thereon. Since the contact area S of the **columnar** terminal 9 and the **solder** ball 12 can be increased, as compared with a conventional one, strength against shearing stress can be enhanced. Furthermore, constricted shape reduces rigidity (makes flexible) and increases resiliency thus enhancing stress relaxing performance.
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L34 ANSWER 5 OF 15 JAPIO COPYRIGHT 2002 JPO

AN 1999-126863 JAPIO
TI WIRING BOARD AND PRODUCTION THEREOF
IN MATSUURA TORU
PA NGK SPARK PLUG CO LTD, JP (CO 000454)
PI JP 11126863 A 19990511 Heisei
AI JP1997-292715 (JP09292715 Heisei) 19971024
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 99, No. 5
AB PURPOSE: TO BE SOLVED:To provide a wiring board having terminals which ensure high connection reliability, and a production method therefor. CONSTITUTION: substantially planar wiring board 10 having first and second faces 1a, 1b comprises a wiring board body 1 made of a composite material of epoxy resin and glass fibers, an **integrated circuit chip** 11 mounted on the first face 1a side, and substantially cylindrical columnar terminals 3 made of Pb-Sn eutectic solder having a height CH larger than the maximum diameter AD formed on the second face 1b side. When the forward end of the columnar terminal 3 is abutted against a fixing pad formed on a fixing board and connected by a **solder**, the **columnar** terminal 3 is bent for a deformation along the second face and elongates/contracts for a deformation caused by the difference in the coefficients of thermal expansion between the **integrated circuit chip** 11 and the wiring board body 1. Consequently, stress is relaxed, and the columnar terminal is not ruptured easily thus enhancing the connection reliability.

L34 ANSWER 6 OF 15 JAPIO COPYRIGHT 2002 JPO
AN 1998-125726 JAPIO
TI SUBSTRATE AND ITS CONNECTION
IN OKA KOICHI
PA FUJI XEROX CO LTD, JP (CO 359761)
PI JP 10125726 A 19980515 Heisei
AI JP1996-277908 (JP08277908 Heisei) 19961021
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 98, No. 5
AB PURPOSE: TO BE SOLVED:To provide a substrate which can beforehand prevent breaking of a connection part caused by a concentrated stress, by shaping connected bumps reliably into such a predetermined configuration as to avoid any concentrated stress, and also to provide a method for connecting the substrate. CONSTITUTION: t, as shown in the drawing (A), an **IC chip** 10 having terminal electrode parts 11 and **columnar** bumps 12C of **solder** formed on the electrode parts 11 is positioned above terminal electrode parts 18 of a circuit substrate 16 with the side of the bumps 12C facing down, the bumps 12C are heated to be melted by reflow, the entire **IC chip** 10 is moved in an arrowed direction 30 until the surface of a protective film 14 covering a terminal electrode 11 side of the **chip** 10 come into contact with the surface of a protective film 20 on the circuit substrate 16, and then the bumps 12C are cooled and fixedly set. As a result, as shown in the drawing (B), the bumps 12C are changed to drum-shaped bumps 12D having the same shape as openings 22 made in the protective film 20.

L34 ANSWER 7 OF 15 JAPIO COPYRIGHT 2002 JPO
AN 1997-232017 JAPIO
TI **CHIP** JUMPER PART
IN TANOGAMI TAKAO; YAMAMOTO YOICHI
PA TAIYO YUDEN CO LTD, JP (CO 359306)
CHUKI SEIKI KK, JP (CO 419550)

PI JP 09232017 A 19970905 Heisei
AI JP1996-214126 (JP08214126 Heisei) 19960726
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 97, No. 9
AB PURPOSE: TO BE SOLVED:To provide a **chip** jumper part from which an insulating coating film and solder plating are not separated and which can be handled similarly to a resistor or a capacitor.
CONSTITUTION: **chip** jumper part is composed of a columnar element assembly 1 composed of hard copper whose end surface corner part is round and whole surface is satin finished surface 2. An insulating coating film 3 being a jumper part is formed in a central circumferential surface part 5 of the **columnar** element assembly 1.
Solder plating layers 4 and 4' are formed on an end part circumferential surface 6 and an end surface 7 in the columnar element assembly 1 except the jumper part.

L34 ANSWER 8 OF 15 JAPIO COPYRIGHT 2002 JPO
AN 1993-129368 JAPIO
TI SEMICONDUCTOR DEVICE
IN SUZUKI KATSUHIKO
PA NEC CORP, JP (CO 000423)
PI JP 05129368 A 19930525 Heisei
AI JP1991-313417 (JP03313417 Heisei) 19911101
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1429, Vol. 17, No. 5, P. 158 (19930909)
AB PURPOSE: To contrive the improvement of the yield of a semiconductor device and the improvement of workability and the reliability of the device by a method wherein in a flip-**chip** connection structure, a proper gap is provided between a circuit board and a **chip**.
CONSTITUTION: A wall, on which the surface of a semiconductor **chip** 7 is abutted, is provided on the periphery of a circuit board 1. **Columnar solder** bumps 6, which are a little higher than this wall, are kept provided on the board 1 and electrodes 8 on the **chip** 7 are connected with electrodes 4 on the board 1 through the bumps 6.

L34 ANSWER 9 OF 15 JAPIO COPYRIGHT 2002 JPO
AN 1993-021517 JAPIO
TI FLIP **CHIP** BONDING METHOD AND SUBSTRATE USED THEREFOR
IN OIKAWA YOICHI; YAMAMOTO TAKUJI
PA FUJITSU LTD, JP (CO 000522)
PI JP 05021517 A 19930129 Heisei
AI JP1991-172078 (JP03172078 Heisei) 19910712
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1376, Vol. 17, No. 292, P. 119 (19930604)
AB PURPOSE: To easily form a **solder** bump in a **columnar** shape in bonding a flip **chip** to a substrate.
CONSTITUTION: A metallic ball 20 is seated in a recessed section 18 formed on a substrate 8, with a soldering material 22 being brought into contact with the ball 20, so that the ball 20 can move to the outside of the section 18 by the surface tension of the material 22 when the material 22 is melted and can get in between an element **chip** 2 and the substrate 8 when solder bumps 6 harden.

L34 ANSWER 10 OF 15 JAPIO COPYRIGHT 2002 JPO
AN 1992-186663 JAPIO
TI MOUNTING STRUCTURE OF SEMICONDUCTOR ELEMENT
IN KIMURA TOSHIHIRO
PA NISSAN MOTOR CO LTD, JP (CO 000399)

PI JP 04186663 A 19920703 Heisei
AI JP1990-312485 (JP02312485 Heisei) 19901117
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1281, Vol. 16, No. 5, P. 17 (19921019)
AB PURPOSE: To facilitate the mounting and improve the reliability in mounting by mounting a heat spreader, where a semiconductor element is joined, to a mounting member through a coupling means capable of mechanical mounting and removal.
CONSTITUTION: A semiconductor element 1 is joined by **solder** 3 onto a **columnar** heat spreader 15. A male screw 15a is made at the periphery of the heat spreader 15, and this male screw 15a is screwed in the female screw 16 made in the specified position of a case 4 doubling as a heat sink. Hereby, the semiconductor element 1 is coupled with the case 4 doubling as a heat sink electrically and mechanically. Moreover, a recess 15b with which a tool such as a driver, etc., engages is made at the surface, where the semiconductor is not joined, of the heat spreader 15. A **chip** part 8, a connector 9 for external connection, etc., are mounted on the wiring board 6, which is arranged to surround the semiconductor element 1. The semiconductor element 1 and the wiring board 6 are connected with each other by a wire 7.

L34 ANSWER 11 OF 15 JAPIO COPYRIGHT 2002 JPO
AN 1990-096343 JAPIO
TI MANUFACTURE OF HYBRID **INTEGRATED CIRCUIT** DEVICE
IN FUKUDA YUTAKA; YAMAKAWA HIROYUKI
PA NIPPON DENSO CO LTD, JP (CO 000426)
PI JP 02096343 A 19900409 Heisei
AI JP1988-248739 (JP63248739 Heisei) 19880930
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 945, Vol. 14, No. 297, P. 143 (19900627)
AB PURPOSE: To reduce variations in a manufacturing process by interposing solid and plate-shaped thermosetting resin between a semiconductor **chip** and a member on which the semiconductor **chip** is mounted, and subjecting the resin to a specific processing.
CONSTITUTION: Thermosetting resin 4 having an open portion by which a solder 3 is received is placed on a substrate 1, and a flip **chip** 5 having a solder bump 6 as an electrode is placed on the thermosetting resin 4. Heat treatment is performed at a temperature higher than a melting point of the solder, and thereafter the temperature is lowered to permit **die** sample to be heated at a temperature higher than a temperature where the thermosetting resin is hardened and lower than the melting point of the solder. Therefore, the solder located at a bonding portion is solidified into a **columnar solder** 7, and the thermosetting resin 4 is first softened into a liquid to fill among the **chip**, the substrate, and the surroundings of the **columnar solder** 7. Hereby, the thermosetting resin 4 can satisfactorily be filled to reduce the variation of resin thickness.

L34 ANSWER 12 OF 15 JAPIO COPYRIGHT 2002 JPO
AN 1989-019640 JAPIO
TI MANUFACTURE OF RIVET TYPE CONTACT
IN SAITO KOICHI
PA TANAKA KIKINZOKU KOGYO KK, JP (CO 399618)
PI JP 01019640 A 19890123 Heisei
AI JP1987-175520 (JP62175520 Heisei) 19870714
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 755, Vol. 13, No. 196, P. 163 (19890510)
AB PURPOSE: To hinder header processing from causing the solder reaching the surface of the contact by forming a conical step at the periphery of the

joint surface of a contact **chip** for jointing with a columnar base with the central part left, brazing the contact **chip** fast to the columnar base, and performing header processing.
CONSTITUTION: With the central part 2a left, a conical step 2b is formed at the periphery of the joint surface of a contact **chip** 2 to provide a contact **chip** 2'. This contact **chip** 2' is **brazed** fast to a **columnar** base 3 with Ag **solder** 4 to provide a clad contact material 5'. This clad contact material 5' is header processed to provide a rivet type contact 6'. At this rivet type contact 6', molten solder 4' stagnates in a ring-shaped recess 7 between the conical step 2b of the contact **chip** 2' and the joint surface of the columnar base 3 when the contact **chip** 2' is **brazed** fast to the **columnar** base 3, and does not float up to the periphery of the contact **chip** 2', and thus the header processing does not cause the solder 4' reaching the surface of the contact.

L34 ANSWER 13 OF 15 JAPIO COPYRIGHT 2002 JPO
AN 1988-062333 JAPIO
TI METHOD FOR SOLDERED JOINT OF FLIP **CHIP**
IN INABA TOYOKAZU; KAMOGAWA TOMOHISA
PA OKI ELECTRIC IND CO LTD, JP (CO 000029)
PI JP 63062333 A 19880318 Showa
AI JP1986-206025 (JP61206025 Showa) 19860903
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 642, Vol. 12, No. 285, P. 123 (19880804)
AB PURPOSE: To form **solder** bumps into a **columnar** form by a method wherein a flux is applied to both of a flip **chip** and a jig and is heated at the temperature of solder fusing or higher and the flip **chip** is so contrived as to be pulled up on the jig side by the surface tension of the flux.
CONSTITUTION: A flip **chip** 12 is previously connected on a circuit substrate 11 through solder bumps 13 by a solder fusion method. Solvent having a surface tension even at a solder fusing temperature, such as a flux 14 for solder connection, is dipped on the upper surface of the flip **chip** 12 and moreover, a U-shaped columnar height control jig 15 is covered thereon, leg parts 15a are arranged in such a way as to abut on the circuit substrate 11 and in this state, the flux is heated at a solder fusing temperature or more. Whereupon, the flip **chip** 12 is attracted to the jig 15 by the surface tension of the flux 14, the solder bump parts are stretched out in a **columnar** form and **columnar solder** bumps 13' are formed. The **solders** of the **columnar solder** bumps 13' are solidified and also, at the state of a temperature before the flux 14 is solidified, the jig 15 is dismantled.

L34 ANSWER 14 OF 15 JAPIO COPYRIGHT 2002 JPO
AN 1985-032349 JAPIO
TI COOLING STRUCTURE OF **INTEGRATED CIRCUIT** PACKAGE
IN TAKAMOTO MITSUO
PA NEC CORP, JP (CO 000423)
PI JP 60032349 A 19850219 Showa
AI JP1983-141631 (JP58141631 Showa) 19830802
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 324, Vol. 9, No. 15, P. 161 (19850625)
AB PURPOSE: To obtain a cooling structure of a liquid cooling system which has low temperature drop and ready maintenance by providing a lower frame opposed to an **integrated circuit** module for placing an **integrated circuit** package on a substrate and an upper

frame cooperating with the lower frame for covering a conduit.
CONSTITUTION: An LSI module 1 and a cooling plate 2 are provided, signal pins 10 are provided on one side surface of a ceramic substrate 4 in the module 1, an LSI package 5 is mounted on the opposite surface side, and a **columnar** heat sink 6 is **soldered**. A base frame 8 and a plate 9 are clamped by a screw 11 to the periphery of the substrate 4. The plate 2 is composed of a conduit 16 for flowing liquid, a lower frame 14 for supporting and protecting the conduit 16, and an upper frame 15. The conduit 16 has expansible diaphragms, D, E, and a tube 19 having an arcuate part J for passing the heat sink 6.

L34 ANSWER 15 OF 15 JAPIO COPYRIGHT 2002 JPO
AN 1983-218148 JAPIO
TI COOLING DEVICE FOR ELECTRONIC PART
IN DOTANI AKIHIRO
PA NEC CORP, JP (CO 000423)
PI JP 58218148 A 19831219 Showa
AI JP1982-101053 (JP57101053 Showa) 19820611
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 234, Vol. 8, No. 661, P. 161 (19840328)
AB PURPOSE: To reduce thermal resistance between the heating electronic part and a heat-dissipator, and to improve the performance of cooling by providing a thermal conductive columnar body fixed to the heating electronic part, a cover member connected to the columnar body and the heat-dissipator, the inside thereof has a piping for cooling.
CONSTITUTION: The thermal conductive columnar body 23 is fixed to the back on the side reverse to the circuit forming surface of a semiconductor **integrated circuit** 22 through soft **soldering**, etc. The thermal conductive **columnar** body 23 is connected to the cover member 25 of excellent thermal conductance through solder 24 of the low melting point. The dissipator 26 of excellent thermal conductance is brought into contact and arranged to the upper surface of the cover member 25. The piping 27 for cooling capable of flowing a liquid for cooling is set up into the dissipator 26. According to such constitution, heat generated in the semiconductor **integrated circuit** 22 is transmitted rapidly to the thermal conductive columnar body 23, the cover member 25 and the dissipator 26, and transmitted and radiated efficiently to the outside of a package by the fluid flowing in the cooling piping 27.

L38 ANSWER 1 OF 4 WPIX (C) 2002 THOMSON DERWENT
AN 2002-168529 [22] WPIX
DNN N2002-129027
TI Bump transfer substrate for manufacture of ball grid array **package**, **chip** size **package**, has solder bump made up of fusible metal or fusible alloy, formed on its surface.
DC U11
PA (KANN) NEC KANSAI LTD
CYC 1
PI JP 2001358160 A 20011226 (200222)* 6p
ADT JP 2001358160 A JP 2000-177759 20000614
PRAI JP 2000-177759 20000614
AB JP2001358160 A UPAB: 20020409
NOVELTY - A solder bump (11) made up of a fusible metal or a fusible alloy, is formed on a **polyimide** film or a flexible resin board (21). The heat resistant temperature of the flexible resin board is more than 200 deg. C. The melting points of the bump are 150-300 deg. C.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for solder bump transfer method.
USE - For manufacture of ball grid array **package** and **chip** size **package**.
ADVANTAGE - Enables pulling several **rows** of the **solder** bumps at a time, as the transfer bump substrate is flexible. Prevents the silicon **chip** being destroyed.
DESCRIPTION OF DRAWING(S) - The figure shows an explanatory drawing of transfer process of solder bump to silicon **chip**.
Solder bump 11
Flexible resin board 21
Dwg.4/6

L38 ANSWER 2 OF 4 WPIX (C) 2002 THOMSON DERWENT
AN 2000-136209 [12] WPIX
DNN N2000-101821 DNC C2000-041680
TI **Integrated circuit** redistribution structure including a redistribution layer.
DC A85 L03 U11
IN CHANG, C; COBARRUVIAZ, M L; LEIBOVITZ, J; SCHOLZ, K D; SWINDLEHURST, S J; YU, P; ZHU, Y Y
PA (HEWP) HEWLETT-PACKARD CO
CYC 1
PI US 6011314 A 20000104 (200012)* 9p
ADT US 6011314 A US 1999-241221 19990201
PRAI US 1999-241221 19990201
AB US 6011314 A UPAB: 20000308
NOVELTY - The structure has conductive pads (110) formed on the active side of an **integrated circuit**. A redistribution layer formed of conductive lines (140), with at least one of them electrically connecting at least one conductive pad to a solder bump received by an under bump material structure (150).
DETAILED DESCRIPTION - An **integrated circuit** redistribution structure includes conductive pads on the active side of an **integrated circuit**. A redistribution layer is formed over the conductive pads and over the substrate and comprises conductive lines with at least one connected to at least one conductive pad. The conductive lines each comprise an adhesion and diffusion barrier layer (142), an electrical conductor layer (144) and a first metallic **protective** layer (146) formed in this order. An under bump material structure is formed over the first metallic **protective**

layer for receiving a solder bump and is electrically connected to at least one conductive line. The under bump material structure comprises a solder wettable metal layer (152) with a second metallic **protective** layer (154) formed over it for receiving the solder bump. At least one conductive line electrically connects at least one conductive pad to the solder bump received by the under bump material structure.

USE - For interconnecting conductive pads of an **integrated circuit** on a silicon substrate (100) to solder bumps formed at the interior of the silicon substrate surface.

ADVANTAGE - The redistribution layer allows solder bumps to be electrically connected to the conductive pads while being formed over the **integrated circuit** at positions different than the locations of the conductive pads.

DESCRIPTION OF DRAWING(S) - The drawing shows the redistribution lines and under bumping material.

Substrate 100
Conductive pad 110
Mechanically **protective** layer 130
Conductive line 140
Diffusion barrier layer 142
Electrical conductor layer 144
Metallic **protective** layer 146
Under bump material structure 150
Solder wettable metal layer 152
Second metallic **protective** layer 154

Dwg.2A,2B/4

L38 ANSWER 3 OF 4 WPIX (C) 2002 THOMSON DERWENT
AN 1998-172371 [16] WPIX
DNN N1998-137085
TI Image pick-up unit for endoscope - has anisotropic electrically conductive adhesive film that connects land of **polyimide** substrate with external lead of TAB tape after signal **line** is **soldered** to another land of **polyimide** substrate.
DC P31 P81 S05 W04
PA (OLYU) OLYMPUS OPTICAL CO LTD
CYC 1
PI JP 10033475 A 19980210 (199816)* 5p
ADT JP 10033475 A JP 1996-193099 19960723
PRAI JP 1996-193099 19960723
AB JP 10033475 A UPAB: 19980421

The unit has a **polyimide** substrate (10) provided with lands (11,12) for connection. The input-output terminal of a CCD bare **chip** (1) is joined to an inner lead (7) of a TAB tape (4). A current carrying part is drawn from the TAB tape to form an external lead (8).

The connection for the external lead and a signal line (9) is formed on the **polyimide** substrate. The signal **line** and a land are **soldered** beforehand. The external lead and another land are connected with the use of an anisotropic electrically conductive adhesive film (13).

ADVANTAGE - Improves weld operativity since junction work of signal line does not need to be soldered immediately. Improves reliability of connection work using anisotropic electrically conductive adhesive film since no heat is generated as in **case** of soldering.

Dwg.1/3

L38 ANSWER 4 OF 4 WPIX (C) 2002 THOMSON DERWENT

AN 1996-169138 [17] WPIX
DNN N1996-142316 DNC C1996-053272
TI Lid for sealing semiconductor **package** - has alpha ray resin cover layer e.g. made from **polyimide** resin, to shield alpha rays emitted from ceramic board.
DC A85 L03 U11
PA (SUMI-N) SUMITOMO KINZOKU CERAMICS KK
CYC 1
PI JP 08051167 A 19960220 (199617)* 10p
ADT JP 08051167 A JP 1994-338089 19941226
PRAI JP 1994-142354 19940531
AB JP 08051167 A UPAB: 19960428
The lid (1) has a solder layer about its circumference part (3) with a ridge **line** between them. A thick **solder** part is formed as a curved structure. An alpha ray cover resin layer (5) covers the alpha rays emitted from a ceramic board (2), set within the solder layer. The **package** sealing is done to seal the semiconductor **chip** mounted to a **chip** mounting part of a semiconductor **package** base.

USE/ADVANTAGE - In LSI and **IC chips**. Eases formation of solder layer. Prevents incorrect mounting of semiconductor **chip**.

Dwg.2/10

L42 ANSWER 1 OF 36 WPIX (C) 2002 THOMSON DERWENT
AN 2002-214995 [27] WPIX
DNN N2002-164600 DNC C2002-065672
TI Electronic component assembling method during burn-in or testing, involves mounting sub-assembly of electronic component and base plate onto test apparatus through input/output connection of base plate.
DC L03 U11
IN FAROOQ, M S; JACKSON, R A; KNICKERBOCKER, S H; RAY, S K
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 6335210 B1 20020101 (200227)* 5p
ADT US 6335210 B1 US 1999-466607 19991217
PRAI US 1999-466607 19991217
AB US 6335210 B UPAB: 20020429
NOVELTY - Electronic component (10) is mounted on base plate (20) having Young's modulus greater than 5 Gpa. The sub-assembly is in turn mounted on test apparatus through an input/output (I/O) connection selected from among a solder ball, **solder** pad, and **solder column**. After testing, if the component is good, the assembly is removed and mounted on a substrate through the I/O connection (12, 22) of the base plate (20).
USE - The method is used for burn-in and/or testing of semiconductor **chips**, capacitors, resistors to be mounted on multichip modules.
ADVANTAGE - The base plate provides an added strength to complex component while it is being tested and also during normal use.
DESCRIPTION OF DRAWING(S) - The figure shows the electronic component secured to base plate forming sub-assembly prior to burn-in and/or testing.
Electronic component 10
I/O connections 12, 22
Baseplate 20
Sub-assembly 23
Dwg.1/3

L42 ANSWER 2 OF 36 WPIX (C) 2002 THOMSON DERWENT
AN 2001-146257 [15] WPIX
DNN N2001-107006
TI Electrical connection method for contact testing of full **wafer** of **chips**, involves applying loading force to cause more than one of nickel columns to form indentations into **wafer** solder balls.
DC S01 U11 V04
IN BEHFAR, A A; MCHERRON, D C; PERRY, C H
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 6174175 B1 20010116 (200115)* 9p
ADT US 6174175 B1 US 1999-301568 19990429
PRAI US 1999-301568 19990429
AB US 6174175 B UPAB: 20010317
NOVELTY - A loading force is applied to a **wafer** (7) so that rigid nickel columns (2) will conductively contact with the solder balls (5) of the **wafer**. The loading force applied is sufficient to cause more than one of the nickel columns to form indentations into the solder balls of the **wafer**.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a high-density Z-B1xis connector.
USE - For contact testing of single **chips** or full **wafer** of **chips**.
ADVANTAGE - Attains good electrical contact between highly dense

opposing sets ot arrays of electrical contact points without requiring alignment.

DESCRIPTION OF DRAWING(S) - The figure shows the explanatory drawing of connector or interposer.

Dwg.4/7

L42 ANSWER 3 OF 36 WPIX (C) 2002 THOMSON DERWENT
AN 2001-025391 [04] WPIX
DNN N2001-019784
TI Area array component, such as in **integrated circuits** solder joint verification laser scan, implements laser technology to determine actual lattice topology and mapping of open joints.
DC S02 S03 U11 V04 X24
IN JAVDAN, R
PA (JAVD-I) JAVDAN R
CYC 1
PI CA 2251511 A1 20000503 (200104)* EN 2p
ADT CA 2251511 A1 CA 1998-2251511 19981103
PRAI CA 1998-2251511 19981103
AB CA 2251511 A UPAB: 20010118

NOVELTY - Narrow laser beams are used to map the inner ball or column topology either by transmission of the laser beam through the lattice at various incident angles, or reflection of laser beam by bouncing it off solder joints to compare the actual paths and determine actual lattice topology, or by Z-direction scan of individual joints in the lattice.

DETAILED DESCRIPTION - Z-direction (components body to substrate direction) scan is carried out for reflection/transmission investigation and matching to computer model of joint, which in addition enables determination of wetting property of joint.

USE - For verification of connections in electronic circuit assemblies, such as between **integrated circuit** (**IC**) and printed circuit board (PCB), where matrix array of solder balls (in BGA, PBGA) or **solder columns** (in CGA,CCGA) are used to attach connections.

ADVANTAGE - Method exhibits reduced cost and duration of verification.

DESCRIPTION OF DRAWING(S) - No Drawings given.

Dwg.0/0

L42 ANSWER 4 OF 36 WPIX (C) 2002 THOMSON DERWENT
AN 2000-655727 [63] WPIX
CR 2000-386328 [31]
DNN N2000-486063
TI Shaving blade for **chip** site dressing, has integral vacuum suctioning unit comprising a passageway terminating in an upstanding wall of wedge-shaped leading edge of the blade tip.
DC P55 P62 X24
IN BURKE, J A; OLSON, D C; TERSIGNI, J E; WOLFE, J S
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 6131794 A 20001017 (200063)* 5p
ADT US 6131794 A US 1997-872951 19970611, Div ex US 1999-266659 19990311
PRAI US 1999-266659 19990311; US 1997-872951 19970611
AB US 6131794 A UPAB: 20001205

NOVELTY - An integral vacuum suctioning unit has a passageway formed in an elongated element (12) of the blade (10). The tip portion (18) of blade has a wedge-shaped cross section forming a thin leading edge extending across elongated blade element. The upper surface of leading edge has a tip standing wall at rearward end. One end of the passageway in the vacuum

suctioning unit, terminates in the upstanding wall.

DETAILED DESCRIPTION - The tip portion of the blade is angled upwardly and forwardly of the longitudinal extent of the elongated blade element. The upwardly angled tip portion subtends an angle within the range of 30-60 deg. , with the longitudinal extend of the elongated blade element. The blade is made of cobalt impregnated, prehardened high speed tool steel.

USE - For **chip** site dressing for removing components from multichip modules. Also for removing solder blade flip **chip**, **solder** balls, **solder columns**, wire bond interconnections, hermetic **solder** seal bands, solder seal pads.

ADVANTAGE - The angle of blade can be readily modified to operate with different top surface architectures of multichip modules. The height of the blade can be accurately controlled, depending on the product type to be processed.

DESCRIPTION OF DRAWING(S) - The figure shows the perspective view of the blade.

Blade 10

Elongated element 12

Tip portion 18

Dwg.1/5

L42 ANSWER 5 OF 36 WPIX (C) 2002 THOMSON DERWENT
AN 2000-136343 [12] WPIX
DNN N2000-101933 DNC C2000-041744
TI **Microelectronic** assembly including an **integrated circuit** component attached to a substrate.
DC L03 U11
IN MORRELL, M J
PA (MOTI) MOTOROLA INC
CYC 1
PI US 6013571 A 20000111 (200012)* 7p
ADT US 6013571 A US 1997-876582 19970616
PRAI US 1997-876582 19970616
AB US 6013571 A UPAB: 20000308

NOVELTY - The method comprises depositing metallic columns (24) onto component bond pads disposed on an **integrated circuit** component (12). The metallic **columns** include a **solder** attachment surface remote from the **integrated circuit** component, and a solder-nonwettable peripheral surface intermediate the solder attachment surface (28) and the component bond pad (32). The metallic columns are formed of a first metal having a first melting temperature. A solder plate (30) is deposited onto each solder attachment surface, the plate being formed of a solder having a second melting temperature that is lower than the first melting temperature. This preassembly is superposed onto a substrate (14) such that each solder plate contacts a corresponding substrate bond pad on the substrate. The solder is reflowed by heating to a temperature above the second melting temperature and below the first melting temperature to bond the metallic column to the substrate bond pad, thereby attaching the **integrated circuit** component to the substrate.

USE - A method for forming a **microelectronic** assembly including an **integrated circuit** component attached to a substrate by columnar interconnections.

ADVANTAGE - The structure provides a predetermined standoff between the component and the substrate, and controlled lateral dimensions between interconnections to avoid shorting.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-sectional view of the **microelectronic** assembly.

Microelectronic assembly 10
Integrated circuit component 12
Substrate 14
Bond pads 16
Metallic columns 24
Solder attachment surface 28
Solder plate 30
Substrate bond pad 32
Solder joint 34
Dwg.3/4

L42 ANSWER 6 OF 36 WPIX (C) 2002 THOMSON DERWENT
AN 2000-136168 [12] WPIX
CR 2001-089798 [59]
DNN N2000-101794
TI BGA socket connector system.
DC S01 U11 V04
IN CAMPBELL, J S; NESKY, R W
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 6010340 A 20000104 (200012)* 9p
ADT US 6010340 A US 1998-34940 19980304
PRAI US 1998-34940 19980304
AB US 6010340 A UPAB: 20010220
NOVELTY - The system forms a separable electrical contact between a first circuit substrate (10) and a second substrate. A dendrite interposer is disposed between the two circuit substrates. A solder body (20c) is disposed between the first circuit substrate and the dendrite interposer. The solder body has a contact end (32c) which engages the dendrite interposer.
USE - For socketing single **chip** or multi-**chip** modules by **solder columns** or balls.
ADVANTAGE - Forms separable and reliable electrical connection between circuit substrates.
DESCRIPTION OF DRAWING(S) - The figure shows a solder ball.
first circuit substrate 10
solder body 20c
contact end 32c
Dwg.7/8

L42 ANSWER 7 OF 36 WPIX (C) 2002 THOMSON DERWENT
AN 2000-022081 [02] WPIX
DNN N2000-016342 DNC C2000-005278
TI Production of multichip module and heat sink cap assembly.
DC L03 U11 V04
IN DIGIACOMO, G; DROFITZ, S S; EDWARDS, D L; GOLAND, D B; GROSS, L D; HERRON, L W; IRUVANTI, S; SHERIF, R A; SHINDE, S L; WOMAC, D J
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 5981310 A 19991109 (200002)* 8p
ADT US 5981310 A US 1998-12071 19980122
PRAI US 1998-12071 19980122
AB US 5981310 A UPAB: 20000112
NOVELTY - A multichip module having an integral heat sink cap is formed by **solder** bonding heat sink **columns** (20) matched to the **chips** (14), with the columns being flexibly interconnected (22) to give a unitary structure.
DETAILED DESCRIPTION - A method of making a multichip module with an integral heat sink cap comprises forming a cap of material having a

similar coefficient of thermal expansion to the multichip substrate (12) and comprising heat sink columns (20) arranged in the same pattern as the **chips** (14) and having a surface which can be bonded to the **chips**. The columns are interconnected by flexible members (22), a conductive film is deposited on at least part of the **chip** surface and the columns and the substrate and cap are assembled with solder between mating portions of the cap and **chips** and between substrate and cap. The solder is then reflowed to bond the cap to substrate and **chips**.

USE - For dissipating heat from high power multichip **integrated circuit** modules.

ADVANTAGE - Cooling capacity is much increased without affecting **chip**-substrate interconnection and can exceed 75 W cm-2.

DESCRIPTION OF DRAWING(S) - An elevation of the assembly is shown.

Substrate 12

Chips 14

Heat sink columns 20

Flexible interconnections 22

Dwg.1/6

L42 ANSWER 8 OF 36 WPIX (C) 2002 THOMSON DERWENT
AN 1999-428703 [36] WPIX
DNN N1999-319025
TI Electrical interconnect assembly for information handling system e.g. computers.
DC T01 V04
IN KEHLEY, G L; MYRTO, G E; SHERMAN, J H
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 5919050 A 19990706 (199936)* 12p
ADT US 5919050 A US 1997-834064 19970414
PRAI US 1997-834064 19970414
AB US 5919050 A UPAB: 19990908

NOVELTY - Electrical interposer (40) with separate contact arrays for contacting arrays of **IC** modules (60) and PCB (30), is provided between **IC** module and PCB. Base has posts extending through holes of PCB, interposer and module. Heads at openings of cam ring (90), press module towards substrate to maintain contact between module and substrate with corresponding interposer contacts.

DETAILED DESCRIPTION - A registration sheet positions the **integrated circuit** module and having module locator holes extending through the sheet. A pressure plate (70) presses the module towards printed circuit board of card. A wave spring (80) with annular ring exerts the pressure on pressure plate and compensates the dimensional variations and deviation from planarity. The module contacts have **solder** balls or **columns**. An INDEPENDENT CLAIM is also included for electrical interconnecting method.

USE - For information handling system e.g. computers, set top boxes.

ADVANTAGE - Since base provides posts that extend through holes of PCB, interposer and modules, when ring is turned on to compress the wave spring and press the circuit module towards PCB the alignment between PCB, interposer and registration are maintained. Since cam ring and annular wave spring exerts force on surface of pressure plate, good electrical connections are made with contacts in array.

DESCRIPTION OF DRAWING(S) - The figure shows an exploded perspective view of electrical interconnect assembly.

PCB 30

Electrical connector 40

IC modules 60

Pressure plate 70
Wave spring 80
Cam ring 90
Dwg.1/12

L42 ANSWER 9 OF 36 WPIX (C) 2002 THOMSON DERWENT
AN 1999-356628 [30] WPIX
DNN N1999-265454 DNC C1999-105415
TI Solder removal from a substrate, e.g. to inspect a semiconductor **chip**.
DC L03 M23 P55 V04 X24
IN JIMAREZ, L J; JIMAREZ, M A
PA (IBMC) INT BUSINESS MACHINES CORP; (JIMA-I) JIMAREZ M A
CYC 1
PI US 5909838 A 19990608 (199930)* 7p
ADT US 5909838 A US 1997-964291 19971104
PRAI US 1997-964291 19971104
AB US 5909838 A UPAB: 20000228
NOVELTY - Copper foil (3) with a microroughened surface (9) is brought adjacent solder (2) on an article (1) by vacuum suction through a hole in a copper block (4). The foil is then heated by conduction through the block using an infrared heat source (7). Some of the solder is melted, and drawn on to the roughened surface. The foil is then withdrawn.
USE - Removing solder from a substrate, e.g. for inspection of a **chip**.
ADVANTAGE - The process is simpler and cheaper than prior art methods.
DESCRIPTION OF DRAWING(S) - The figure shows the apparatus during solder removal.
article 1
solder bumps 2
foil 3
rework head 4
vacuum tube 5
hot air nozzle 6
infrared heat lamp 7
support 8
roughened surface 9
Dwg.1/3

L42 ANSWER 10 OF 36 WPIX (C) 2002 THOMSON DERWENT
AN 1998-498206 [43] WPIX
DNN N1998-389225 DNC C1998-150175
TI Accurately sized solder bump production - using delimiting oxide brim formed by oxidising solder-stop layer.
DC A85 L03 U11
IN DUTZI, J; HAUER, H; KUKE, A
PA (BOSC) BOSCH GMBH ROBERT
CYC 24
PI EP 867931 A1 19980930 (199843)* DE 10p
R: AL AT BE CH DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
DE 19712219 A1 19981001 (199845)
ADT EP 867931 A1 EP 1997-120315 19971120; DE 19712219 A1 DE 1997-19712219 19970324
PRAI DE 1997-19712219 19970324
AB EP 867931 A UPAB: 19981028
In a method of producing solder bumps of specific size by applying a solder-wettable contact layer (3, 13) onto a substrate (1) and then

structuring and remelting cylindrical **solder columns** on the contact layer to form a solder bump (5, 15) of spherical cap shape, the novelty comprises (a) coating the contact layer (3, 13) with a non-solder-wettable, oxidisable solder-stop layer (4, 14) having openings (6, 16) of predetermined size; and (b) heat treating the substrate together with all the applied layers, prior to structuring the **solder columns**, in air to form a non-solder-wettable oxide layer brim (8) in the transition region between the solder-stop layer (4, 14) and the contact layer (3, 13) by lateral diffusion of the oxide of the solder-stop layer. A polyimide layer may be applied onto the solder-stop layer for insulation purposes.

USE - The bumps are useful for mounting and simultaneously contacting of electronic and optoelectronic **chips** on a board or substrate.

ADVANTAGE - The method provides very precise lateral delimiting of the solder bump in a simple and rapid manner.

Dwg.1/4

L42 ANSWER 11 OF 36 WPIX (C) 2002 THOMSON DERWENT
AN 1998-229929 [20] WPIX
DNN N1998-182079
TI Low-profile semiconductor device having first level interconnects through an interposer - uses interposer to connect an active surface of **die** to conductive traces on top surface of substrate.
DC U11
IN DJENNAS, F; JOINER, B A; STERLIN, W
PA (MOTI) MOTOROLA INC
CYC 1
PI US 5734201 A 19980331 (199820)* 7p
ADT US 5734201 A Cont of US 1993-149499 19931109, US 1994-328978 19941021
PRAI US 1993-149499 19931109; US 1994-328978 19941021
AB US 5734201 A UPAB: 19980520

A low profile semiconductor device (24) is manufactured by mounting a semiconductor **die** (26) on to a substrate (28) using an interposer (30). The interposer couples an active surface (32) of the **die** (26) to conductive traces (33) on the top surface of the substrate. The interposer is directionally conductive so that electrical conductivity is limited to the z-direction through thickness of the interposer.

The interposer both affixes the **die** to the substrate and provides the first level of interconnects for the device. The inactive surface (36) of the **die** can be exposed for efficient thermal dissipation. An optional heat spreader (50) may be added for increased thermal management. The device may be overmolded, glob-topped, capped, or unencapsulated. Separate **die**-attach and wire bonding processes are eliminated. A second level of interconnects are provided by either **solder** balls (38), **solder columns** (44), or pins (64).

USE - For electronics industry.

ADVANTAGE - Reduced packaging costs.

Dwg.6,7/7

L42 ANSWER 12 OF 36 WPIX (C) 2002 THOMSON DERWENT
AN 1998-103292 [10] WPIX
DNN N1998-082841 DNC C1998-034109
TI System for connecting **chip** substrate to PCB - uses array of narrow **solder columns** between pads on substrate and PCB and wider **solder columns** at periphery to provide support reinforcement when heat sink is attached.
DC L03 M23 U11 V04

IN DOCKERTY, R C; FRAGA, R M; RAMIREZ, C N; RAY, S K; ROBBINS, G J
PA (IBMC) INT BUSINESS MACHINES CORP; (IBMC) IBM CORP
CYC 25
PI EP 822738 A2 19980204 (199810)* EN 9p
R: AL AT BE CH DE DK ES FI FR GB GR IE IT LI LT LU LV MC NL PT RO SE SI
JP 10092983 A 19980410 (199825) 9p
KR 98013574 A 19980430 (199917)
KR 264638 B1 20000901 (200134)
ADT EP 822738 A2 EP 1997-305034 19970709; JP 10092983 A JP 1997-190974 19970716; KR 98013574 A KR 1997-21697 19970529; KR 264638 B1 KR 1997-21697 19970529
PRAI US 1996-688073 19960729
AB EP 822738 A UPAB: 19980316
The system for connecting a low expansion substrate (1) to a higher expansion PCB (6) using **solder columns** (7) and reflow bonding comprises: (i) a support apparatus formed of an array of high-melting **solder columns** (7) attached to pads (3) on the substrate (1); (ii) a set of high melting **solder columns** (14) of greater cross-section than the first columns (7) by a factor of five or more attached to pads (13) at the substrate perimeter; and (iii) connections between the respective columns (7,14) and their pads (4,16) on the PCB using reflowed low melting solder (17).

Also claimed is a process for connecting the substrate to the PCB via the above system, with a heat sink being further thermally attached to the **chip** on the top surface of the substrate.

ADVANTAGE - The substrate bonding arrangement allows a heat sink to be attached to the **chip** without causing undue stress to the **solder columns**. The peripheral reinforcing **solder columns** maintain spacing and structural integrity in the presence of vibration and temperature variation.
Dwg.2/4

L42 ANSWER 13 OF 36 WPIX (C) 2002 THOMSON DERWENT
AN 1997-502441 [46] WPIX
DNN N1997-418828
TI Hybrid multi-**chip** module assembly - has **solder columns** compliant to absorb any dimensional changes which occurs when MCM-L and MCM-D type structures are subjected to heat.
DC U11 U14
IN LUNSFORD, D; SWAMY, D
PA (DELL-N) DELL USA LP; (SWAM-I) SWAMY D
CYC 1
PI US 5675183 A 19971007 (199746)* 7p
ADT US 5675183 A US 1995-501331 19950712
PRAI US 1995-501331 19950712
AB US 5675183 A UPAB: 19990210
The multi-**chip** module comprises an MCM-D with a planar side with several spaced semiconductor **chips** mounted on. A series of spaced first electrically conductive pads are mounted on this side, outwardly of the spaced number of semiconductor **chips**. A spaced series of first electrically conductive lead members carried on the MCM-D body portion and electrically couple the first electrically conductive pads to the semiconductor **chips**. An MCM-L has a body portion with a generally planar second side, a spaced series of second electrically conductive pads mounted on the second side, and a spaced series of second electrically conductive lead members carried on the MCM-L body portion and electrically coupling the second electrically conductive pads.

The MCM-D and MCM-L are in an orientation such that the first and second sides are in a spaced apart, parallel, facing relationship with the first electrically conductive pads. A spaced series of electrically conductive column members are transversely disposed between the first and second sides. The column members support the MCM-D and MCM-L in the orientation, with the opposite sides of each column member being conductively secured to a facing pair of the first and second electrically conductive pads. One of the opposite ends of each column member is conductively secured to one of the first electrically conductive pads with relatively high melting point solder.

USE/ADVANTAGE - Combines best features of MCM-L and MCM-D technology.

Dwg.4/5

L42 ANSWER 14 OF 36 WPIX (C) 2002 THOMSON DERWENT
AN 1997-332061 [30] WPIX
DNN N1997-275653 DNC C1997-106537
TI Fabrication of **solder column** grid arrays - for mounting **microelectronic integrated circuits** on circuit boards.
DC L03 M23 U11
IN LIANG, D; SCHNEIDER, M R
PA (LSIL-N) LSI LOGIC CORP
CYC 7
PI US 5639696 A 19970617 (199730)* 7p
EP 788159 A2 19970806 (199736) EN 8p
R: DE FR GB IT NL
JP 09214121 A 19970815 (199743) 7p
ADT US 5639696 A US 1996-595022 19960131; EP 788159 A2 EP 1996-307734 19961025; JP 09214121 A JP 1996-285420 19961028
PRAI US 1996-595022 19960131
AB US 5639696 A UPAB: 19970723
A method of forming an array of electrically conductive columns for interconnecting first and second **microelectronic** devices comprises: (a) interconnecting the two devices with an array of re-flowable electrically conductive balls that correspond to the columns; (b) applying heat to cause the balls to reflow; (c) causing relative movement of the devices away from each other so that the balls are stretched to form columns; and (d) removing the heat.

USE - Surface mounting of **IC** s on circuit boards.

ADVANTAGE - The time consuming process of inserting **solder columns** individually into holes in a graphite fixture or boat is eliminated.

Dwg.8/9

L42 ANSWER 15 OF 36 WPIX (C) 2002 THOMSON DERWENT
AN 1997-244559 [22] WPIX
CR 1997-153209 [14]; 1998-192268 [17]
DNN N1997-201751
TI Direct customised thermally conductive path for semiconductor element and thermal cap - has at least two non-metallic thermally conductive materials, e.g. thermal oil or paste, directly present between respective semiconductor elements and thermal cap.
DC U11 V04
IN COURTNEY, M G; EDWARDS, D L; FAHEY, A J; HOPPER, G S; IRUVANTI, S; JONES, C F; MESSINA, G P; SHERIF, R A
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 5623394 A 19970422 (199722)* 8p
ADT US 5623394 A Cont of US 1994-349232 19941205, US 1996-690883 19960802

PRAI US 1994-349232 19941205; US 1996-690883 19960802
AB US 5623394 A UPAB: 19980428
The apparatus includes at least two non-metallic thermally conductive materials that are directly present between respective semiconductor elements and a thermal cap. One material is either thermal oil, thermal paste, thermal grease or thermal compound.
The thermal conductivity of the two materials are mutually different from one another and the heat generation of the respective semiconductor elements are mutually different one another. A portion of at least one semiconductor is secured a substrate via C4, **solder** ball, **solder column**, or **solder**.
ADVANTAGE - Provides customized cooling of MCM by using several thermally conductive materials.
Dwg.2/4

L42 ANSWER 16 OF 36 WPIX (C) 2002 THOMSON DERWENT
AN 1997-138273 [13] WPIX
DNN N1997-114269
TI Metal bump structure for electronic circuit of flip **chip** configuration - has soft solder bump that is layered on core bump which is provided on column like part made of metal.
DC U11
PA (NIUR) SHIN NIPPON MUSEN KK
CYC 1
PI JP 09017795 A 19970117 (199713)* 4p
ADT JP 09017795 A JP 1995-187887 19950630
PRAI JP 1995-187887 19950630
AB JP 09017795 A UPAB: 19970326
The structure consists of a semiconductor **chip** on which an electrode pad (1) is provided. A metal barrier (2) is layered on the electrode pad.
A column like part (3) made of metal is installed on the metal barrier. A core bump (4) is layered on the column like part. Then, a soft solder bump (5) is layered on the core bump.
ADVANTAGE - Reduces installation process, thereby reducing cost of metal bump structure. Prevents generation of crack in bump due to heat stress.
Dwg.1/7

L42 ANSWER 17 OF 36 WPIX (C) 2002 THOMSON DERWENT
AN 1996-276199 [28] WPIX
DNN N1996-232402 DNC C1996-087590
TI Mfr. of hybrid **integrated circuits** - includes formation of photo-resist on aluminium and removal of aluminium to leave assembly **columns** on carrier, **soldered** to contact areas of **columns** formed on substrate.
DC A85 L03 M14 M23 U14 V04
IN GOLOBAR, E G; PLAKSIN, G A; SALTYKOV, V V
PA (GOLO-I) GOLOBAR E G
CYC 1
PI RU 2047948 C1 19951110 (199628)* 4p
ADT RU 2047948 C1 RU 1994-10740 19940329
PRAI RU 1994-10740 19940329
AB RU 2047948 C UPAB: 19960719
Mfr. of hybrid **integrated circuits** includes forming of assembly columns on contact areas on dielectric substrate by application of photo-resistive mask on polyamide carrier with aluminium foil according to mirror pattern of contact areas on substrate, etching of aluminium, removal of mask and forming of contact areas, followed by soldering of

contact areas on substrate and carrier.
USE/ADVANTAGE -Mfr. of hybrid **integrated circuits**
. Extended class of used components. Bul. 31/10.11.95
Dwg.4/7

L42 ANSWER 18 OF 36 WPIX (C) 2002 THOMSON DERWENT
AN 1993-072463 [09] WPIX
DNN N1993-055471
TI Flip-**chip** bonding method for electrically and mechanically connecting element **chip** with substrate - solidifying solder bump with metallic ball between element **chip** and substrate for controlling space by ball, resulting in **column** shaped **solder** bump formation NoAbstract.
DC U11
PA (FUIT) FUJITSU LTD
CYC 1
PI JP 05021517 A 19930129 (199309)* 6p
ADT JP 05021517 A JP 1991-172078 19910712
PRAI JP 1991-172078 19910712

L42 ANSWER 19 OF 36 WPIX (C) 2002 THOMSON DERWENT
AN 1992-107884 [14] WPIX
TI Semiconductor **chip** installation structure on circuit board - has metal **column** in each **solder** joint NoAbstract Dwg 1/3.
DC U11
PA (HITA) HITACHI LTD
CYC 1
PI JP 04007849 A 19920113 (199214)* 3p
ADT JP 04007849 A JP 1990-107594 19900425
PRAI JP 1990-107594 19900425

L42 ANSWER 20 OF 36 WPIX (C) 2002 THOMSON DERWENT
AN 1988-255069 [36] WPIX
DNN N1988-193649
TI Solder ball for semiconductor **chip** - has height increased so that stress caused by difference in thermal expansion between **chip** and substrate is minimised.
DC U11
PA (ANON) ANONYMOUS
CYC 1
PI RD 291011 A 19880710 (198836)* 1p
PRAI RD 1988-291011 19880620
AB RD 291011 A UPAB: 19930923
A substrate has a solder dam (F) over a substrate conductor (G). The **chip** pad site substrate conductor (G) is then tinned with a low temperature solder alloy (A) to form the base for a **chip** pad **solder column**. Next, a high melt **solder** alloy (B) is evaporated or electroplated on top of the tinning solder (A) to form a solder colum (AB). Finally, another layer of low melt solder alloy (A) is evaporated or electroplated on top of the **solder column** (AB) to form **solder column** (ABA').
The composite structure is reflowed at **chip** joining time with a temperature appropriate for low melting solder (A) but below that of the high melt temperature of solder (B). The second alloy (B) retains is geometry and, therefore, the height of the column is retained. Also, by virtue of the lower joining temperature used the **chip**'s solder ball (D), which is also composed of the high melt solder alloy, retains its geometry.

1/1

L42 ANSWER 21 OF 36 WPIX (C) 2002 THOMSON DERWENT
AN 1987-355362 [50] WPIX
DNN N1987-266233 DNC C1987-152094
TI Depositing uniform drops of solder on substrates - by passing a squeegee over a diaphragm behind a **die**.
DC L03 M23 P42 U11 X24
PA (DENN-I) DENNIS R K
CYC 1
PI US 4710399 A 19871201 (198750)* 10p
ADT US 4710399 A US 1986-902785 19860902
PRAI US 1986-902785 19860902
AB US 4710399 A UPAB: 19930922
Substrate for semi-conductors pass along a guide, below a head which deposits dots of solder paste in a predetermd. pattern on the substrate. The head reciprocates into a depositing position close to the substrate. Pressure is applied to the solder by a squeegee moved across a diaphragm enclosing solder paste behind a **die** producing the required pattern of dots. When the ends of the **solder columns** produced adhere to the substrate the head is raised, and the pressure on the solder simultaneously released. Discharge ceases and columns separate from the dots. The substrate is removed and a fresh one replaces it.
USE/ADVANTAGE - This method can be used to deposit small drops of solder paste in close rows or patterns as required for modern semi-conductor devices. The drops and the spacing can be accurately controlled, without bridging between adjacent drops. The spacing can be much closer than with tubular dispensers, where the dispensed wall thickness is a limitation.
3/10

L42 ANSWER 22 OF 36 WPIX (C) 2002 THOMSON DERWENT
AN 1987-184726 [26] WPIX
DNN N1987-138223
TI **Chip** carrier alignment device and alignment method - has frame and support which are snapped together using system of pins and crenellations.
DC P56 U11 V04
IN GRASSAUER, W K
PA (RAYC) RAYCHEM CORP
CYC 14
PI US 4646435 A 19870303 (198726)* 8p
EP 217678 A 19870408 (198729) EN
R: AT BE CM DE ES FR GB GR IT NL SE
EP 217678 B1 19920909 (199237) EN 11p
R: AT BE CH DE ES FR GB GR IT LI NL SE
DE 3686693 G 19921015 (199243)
ADT US 4646435 A US 1985-784406 19851004; EP 217678 A EP 1986-307686 19861006; EP 217678 B1 EP 1986-307686 19861006; DE 3686693 G DE 1986-3686693 19861006, EP 1986-307686 19861006
FDT DE 3686693 G Based on EP 217678
PRAI US 1985-784406 19851004
AB US 4646435 A UPAB: 19930922
The castellated **chip** carrier alignment device for printed circuit boards or other **chip** carriers compressively engages the castellations in the **chip** carrier, providing precise alignment and positioning of the **chip** carriers relative to other components with which it is assembled.
The device is used with a **solder column** placement

device to produce a preleaded castellated **chip** carrier. The **chip** carrier consists of a frame, a device for compressively engaging one or more of the castellations.

ADVANTAGE - Facilitates alignment of various **chip** carrier types.

1/4

L42 ANSWER 23 OF 36 WPIX (C) 2002 THOMSON DERWENT
AN 1987-023933 [04] WPIX
DNN N1987-018098 DNC C1987-009896
TI Bonding electronic components - using preformed structurally supported **solder columns** with retaining plate to form resilient joints.
DC L02 M23 P55 U11 U14 V04
IN ALLEN, L J; CHERIAN, G; DIAZ, S H
PA (RAYC) RAYCHEM CORP
CYC 1
PI GB 2177641 A 19870128 (198704)*
GB 2177641 B 19880210 (198806)
ADT GB 2177641 A GB 1984-18885 19840702; GB 2177641 B GB 1986-18885 19850713
PRAI US 1983-509684 19830630; US 1984-610077 19840514
AB GB 2177641 A UPAB: 19930922
Appts. comprises preformed structurally supported **solder columns**, predrilled **solder column** support and locating plate, electronic components.

Preformed **solder columns** structurally supported by wound wire or tape and/or filler metal and positioned in a retaining plate, predrilled to match locating positions on electronic components to be **soldered** together. Retaining plate and **columns** are positioned between the components, and the columns heated to bond the components together. Components can be bonded individually or simultaneously and retaining plate can be removed after bonding or left in position.

USE/ADVANTAGE - The appts. and method is useful for bonding together electronic components, especially **chips** and **chip** carriers to p.cb's, permitting precise location of a predetermined quantity of solder forming resilient joints, the reinforced **solder columns** used for bonding retaining their shape during heating.

14B/14

L42 ANSWER 24 OF 36 WPIX (C) 2002 THOMSON DERWENT
AN 1986-219931 [34] WPIX
DNN N1986-164164 DNC C1986-094671
TI Forming solder connections between a **chip** and a substrate - by forming **solder columns** in dams of insulating material at the connection points.
DC A23 A85 L03 U11 U14
IN BLAKESLEE, M C; CHANCE, D A; EASTMAN, D E; GNTEWEK, J J; HO, C W; LEVINE, E N; ORDONEZ, J E; REILEY, T C
PA (IBMC) IBM CORP
CYC 4
PI EP 191434 A 19860820 (198634)* EN 14p
R: DE FR GB
JP 61188942 A 19860822 (198640)
JP 61203648 A 19860909 (198642)
EP 191434 B 19910116 (199103)
R: DE FR GB
DE 3676832 G 19910221 (199109)
ADT EP 191434 A EP 1986-101606 19860207; JP 61188942 A JP 1985-204596

19850918; JP 61203648 A JP 1986-4457 19860114
PRAI US 1985-702199 19850215; US 1985-702296 19850215
AB EP 191434 A UPAB: 19930922
Controlled collapse connections are formed between a **chip** having a surface matrix of connection points and a substrate having a corresponding matrix by: forming a dam of insulating material around at least some of thecnection points; supplying molten solder into the dams; cooling it to form **solder columns**; positioning **chip** and substrate; and heating to melt the solder and form collapsed connections, the dam material being such that the dam and solder separate on cooling so as to permit flexing of the **solder columns**. Dam material is pref. a polyimide or a ceramic.
ADVANTAGE - Method permits greater connections density by enabling longer **solder columns** to be used with freedom to flex without danger of shorting.
9/22

L42 ANSWER 25 OF 36 WPIX (C) 2002 THOMSON DERWENT
AN 1986-019159 [03] WPIX
DNN N1986-013985 DNC C1986-008228
TI **Solder column** extension - in which taller **solder** structures are achieved by evaporating metal core onto each contact site.
DC L03 U11
PA (ANON) ANONYMOUS
CYC 1
PI RD 260050 A 19851210 (198603)*
PRAI RD 1985-260050 19851120
AB RD 260050 A UPAB: 19930922
Taller solder structures are achieved by first evaporating onto each contact site a metal core that is unaffected by subsequent processing temp. and then adding a solder coating. The use of the metal core composite replaces polymer dams and eliminates the crevice and corrosion problems associated with said dams.
A metal core 1, such as copper, is evaporated onto the center of each ball limiting metallurgy (BLM) site 2 of a circuit substrate 3 leaving an insulative layer 4. Solder 5 is evaporated onto each BLM site and reflowed to coat core 1. A circuit **chip** can then be placed on the solder-coated cores and the solder reflowed to join the **chip** and substrate. The metal of core 1 is selected to have a melting temp. above the temps. of subsequent processing steps and will maintain the original height support the **chip** at the desired level.

L42 ANSWER 26 OF 36 WPIX (C) 2002 THOMSON DERWENT
AN 1985-191833 [32] WPIX
DNN N1985-143953
TI Compliant interconnection of leadless **chips** to PCB - using high temperature tin-lead alloy interconnections engaged with plate.
DC U11 V04
IN PAUZA, W V
PA (AMPI) AMP INC
CYC 7
PI EP 150928 A 19850807 (198532)* EN 45p
R: BE DE FR GB IT NL
JP 60239047 A 19851127 (198603)
ADT EP 150928 A EP 1985-300149 19850109; JP 60239047 A JP 1985-16386 19850130
PRAI US 1984-575100 19840130; US 1984-671365 19841114
AB EP 150928 A UPAB: 19930925
The device includes a number of spaced, individual interconnect-tions (31)

extending on both sides of and lockingly engaged with, a plate (25). The plate is made of a flexible, nonelastic dielectric material. The interconnections include columnar portions (31a) on each side of the plate and a vertically offset second columnar portion connected to the first portion by a member (31e).

The interconnections are made of cast **solder columns** and are spaced in from the edges of the plate, and a number of apertures are provided interior of the interconnections. A free end of at least one **solder column** extends beyond the free end of another.

ADVANTAGE - Improved performance to vibrational and temperature cycling stresses. Suitable for high speed mounting to thermal coefficient of expansion differing **chip** carriers.

3/14

L42 ANSWER 27 OF 36 WPIX (C) 2002 THOMSON DERWENT
AN 1981-38730D [22] WPIX
TI Semiconductor **chip** mounting structure - having the **chip** mounted on **solder columns** on the substrate.
DC L03 U11
IN OSHIMA, M; SATOH, R
PA (HITA) HITACHI LTD
CYC 2
PI GB 2062963 A 19810528 (198122)*
DE 3042085 A 19810604 (198124)
GB 2062963 B 19840523 (198421)
DE 3042085 C 19840913 (198438)
ADT GB 2062963 A GB 1980-35586 19801105; DE 3042085 A DE 1980-3042085 19801107
PRAI JP 1979-155903U 19791112
AB GB 2062963 A UPAB: 19930915
Semiconductor **chip** (21) is mounted on a circuit board (24) by means of at least one bonding column (23) of circular cylinder or sandglass form extending between an electrode (22) on the semiconductor **chip** and an electrode (25) on the circuit board with at least one spacer (33) made of solder, which is provided on an isolated pad (34) on the circuit board, which does not wet the semiconductor **chip**, and which keeps the semiconductor **chip** spaced from the circuit board. The spacer is of a solder having a higher m.pt. than that of the connector column.

The **chip** is soldered to the circuit board at all joining points with high work efficiency free from drawback of previous methods and without generation of lateral or rotational forces during the soldering which can displace the **chip**.

L42 ANSWER 28 OF 36 WPIX (C) 2002 THOMSON DERWENT
AN 1981-E9476D [22] WPIX
TI Removal of semiconductor **chip** from substrate - by gas cooling to embrittle solder and twisting to shear solder.
DC P55 U11 U14
IN SHARIFF, R S
PA (IBMC) IBM CORP
CYC 4
PI EP 28700 A 19810520 (198122)* EN
R: DE FR GB
US 4274576 A 19810623 (198128)
EP 28700 B 19830504 (198319) EN
R: DE FR GB
DE 3062975 G 19830609 (198324)
PRAI US 1979-93321 19791113

AB EP 28700 A UPAB: 19930915
Semiconductor **chip** (16a) mounted on a substrate (10) by a number of **solder columns** (18) is detached by chilling the columns to cause their embrittlement, rupturing the columns by slight movement of the **chip** relative the substrate, and subsequently removing the **chip** from the substrate.

Columns are cooled by feeding a cooled liquefied gas through a conduit onto the side of the substrate opposite that to which the columns are attached, via a shroud (22) which shields the substrate from the cooling substance..

Removal of a defective **chip** from a substrate supporting a large number of **chips**. **Chips** are removed without distortion of the **solder columns** making the removal of the remainder of the column much easier.

L42 ANSWER 29 OF 36 WPIX (C) 2002 THOMSON DERWENT
AN 1980-L2031C [47] WPIX
TI **Chip** site dressing system - has device for abrading **solder columns** projecting through holes in mask while pressing against mask.
DC P54 U14
IN MAKHIJANI, M P
PA (IBMC) IBM CORP
CYC 4
PI EP 18557 A 19801112 (198047)* EN
R: DE FR GB
US 4321738 A 19820330 (198215)
EP 18557 B 19820623 (198226) EN
R: DE FR GB
DE 3060573 G 19820812 (198233)
PRAI US 1979-36912 19790507
AB EP 18557 B UPAB: 19930902
The system is for dressing a **chip** site on a ceramic substrate (11) from which a **chip** previously joined to it by solder joints has been removed so as to leave a pattern of **solder columns** (12) on the substrate. The substrate is received at a work station where there is a flexible mask (10) having holes (18) arranged in a pattern corresp. to the **solder columns**, the mask having a uniform thickness corresp. to the heights to which the **solder columns** are to be dressed and being of harder material than the **solder columns**.

A mechanism is provided for placing the mask on the **chip** site with the **solder columns** extending through the holes. An abrading mechanism (24) then scrapes away excess **solder** from the **columns** until the heights of the columns equal the thickness of the mask. The scrapping is performed by pressing the abrading mechanism against the other surface of the mask so as to flex the mask at least approx. conformity with any uneven portions of the surface of the substrate.

L42 ANSWER 30 OF 36 JAPIO COPYRIGHT 2002 JPO
AN 2001-282146 JAPIO
TI LAMINATED DISPLAY PANEL AND METHOD FOR MANUFACTURING THE SAME, HOLDING DEVICE, COMPRESSION BONDING JIG AS WELL AS DRIVE ELEMENT PACKAGING METHOD
IN UEDA MASAHIDE; FURUKAWA KEIICHI; OKADA MASAKAZU; YASUTOMI HIDEO
PA MINOLTA CO LTD
PI JP 2001282146 A 20011012 Heisei
AI JP2000-099599 (JP2000099599 Heisei) 20000331
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2001

AB PROBLEM TO BE SOLVED: To provide a laminated display panel which is formed by laminating a plurality of panel elements and allows the easy packaging of driving **ICs** and the connection of junction substrates after laminating the panel elements.
SOLUTION: The display panel DP 1 laminated with the three panel elements PEb, PEg and PEr. A brazing substrate Sbr formed with **brazing** electrodes, **column** substrate Sbc formed with the **column** substrate, **column** substrate Sgc, **brazing** substrate Sgr, **brazing** substrate Srr and **column** substrate Src are laminated in this order. The extension directions of connecting segments SbrC and SgcC for packaging the driving **ICs** and are made the same. The extension directions of connecting segments SgrC and SrrC of the adjacent substrates are made the same. The extension direction of the connecting segment SbrC, the extension direction of the connecting segment SbcC, the extension direction of the connecting segment SgrC and the extension direction of the connecting segment SrcC are offset by 90° each in this order. The electrode forming surfaces of all the connecting segments are exposed.

L42 ANSWER 31 OF 36 JAPIO COPYRIGHT 2002 JPO
AN 1998-163413 JAPIO
TI **MICROELECTRONIC** PACKAGING USING ARCHED **SOLDER COLUMNS**
IN RINNE GLENN A; DEANE PHILIP A
PA MCNC, US (CO)
PI JP 10163413 A 19980619 Heisei
AI JP1997-138944 (JP09138944 Heisei) 19970528
PRAI US 1996-654539 19960529

L42 ANSWER 32 OF 36 JAPIO COPYRIGHT 2002 JPO
AN 1997-214121 JAPIO
TI **MICROELECTRONICS INTEGRATED CIRCUIT** MOUNTED ON CIRCUIT BOARD HAVING COLUMN-GRID-ARRAY MUTUAL CONNECTION USING **SOLDER**, AND FORMING METHOD OF **COLUMN**-GRID-ARRAY
IN DESHIIN RIYAN; MAAKU AARU SHIYUNAIDAA
PA LSI LOGIC CORP, US (CO)
PI JP 09214121 A 19970815 Heisei
AI JP1996-285420 (JP08285420 Heisei) 19961028
PRAI US 1996-595022 19960131

L42 ANSWER 33 OF 36 JAPIO COPYRIGHT 2002 JPO
AN 1995-218926 JAPIO
TI DISPLAY DEVICE
IN TAMURA MASANORI; YAMASHITA OSAMU; ISOBE MASAYOSHI
PA SANYO ELECTRIC CO LTD, JP (CO 000188)
TOTTORI SANYO ELECTRIC CO LTD, JP (CO 323436)
PI JP 07218926 A 19950818 Heisei
AI JP1994-11085 (JP06011085 Heisei) 19940202
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 95, No. 8
AB PURPOSE: To surely connect a substrate and a driving element even when the electrode of a terminal part is damaged by connecting both the terminals with a specified connecting agent between the substrate of a display and the respective terminal parts of the driving element.
CONSTITUTION: A substrate 1 of a liquid crystal display or the like is exposed on the surface of a pedestal 11 of a glass panel or the like, composed of a transparent electrode and equipped with a terminal part (area) 2 arranged with terminals 12 in a line. On the other hand, a

driving element 3 for driving a display such as the liquid crystal display is provided with an **integrated circuit** element 32 in a film-shaped supporter 31 and arranged with terminal part electrodes 33 in a line composed of a tongue-shaped metal foil set body such as copper foil. Further, an adhesive 4 generally called anisotropic conductive material is mixed with an adhesive resin agent so as to obliquely arrange the **column** of **soldering** particles and by applying pressure in a direction of thickness, electric conduction is provided in the direction of thickness but no electric conduction is provided in a breadthwise direction, namely, in a direction of a plane crossing the direction of thickness. Then, the terminal part 2 is connected through the connecting agent 4 to the terminal part electrodes 33 of the driving element.

L42 ANSWER 34 OF 36 JAPIO COPYRIGHT 2002 JPO
AN 1992-007849 JAPIO
TI PACKAGING STRUCTURE FOR SEMICONDUCTOR ELEMENT
IN DOI HIROAKI; HATSUDA TOSHIO; OGURO TAKAHIRO; HAYASHIDA TETSUYA
PA HITACHI LTD, JP (CO 000510)
PI JP 04007849 A 19920113 Heisei
AI JP1990-107594 (JP02107594 Heisei) 19900425
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1190, Vol. 16, No. 154, P. 43 (19920415)
AB PURPOSE: To moderate strain of connecting solder by constructing the connecting section between a semiconductor element and a wiring board by using **solder** material having metallic **columns** inside.
CONSTITUTION: An Si **chip** 1 is connected to a wiring board 2 through metallic pins, and these three elements are soldered using connecting solder 3. The metallic pins 5 are made by cutting metallic wire into pieces having a constant length. With this, the difference in thermal expansion between the Si **chip** and the wiring board is absorbed by not only the connecting **solder**, but bending of metallic **columns**, thereby moderating the strain of the connecting solder.

L42 ANSWER 35 OF 36 JAPIO COPYRIGHT 2002 JPO
AN 1987-279645 JAPIO
TI METHOD FOR SOLDER CONNECTION
IN TANAKA HIROYUKI; SATO RYOHEI
PA HITACHI LTD, JP (CO 000510)
PI JP 62279645 A 19871204 Showa
AI JP1986-121028 (JP61121028 Showa) 19860528
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 611, Vol. 12, No. 168, P. 95 (19880520)
AB PURPOSE: To connect a semiconductor **chip** with a printed circuit board by preventing the deterioration of the semiconductor **chip** due to heat by locally heating a low-melting-point solder of an irregular plane of positioning **solder columns** after engaging the irregular plane of the positioning **solder columns** respectively formed on a semiconductor **chip** with a printed circuit board.
CONSTITUTION: Positioning **solder columns** 6 are connected to electrodes 5 of a semiconductor **chip** 3 and of printed circuit board 4 respectively with a low-melting-point solder 2'. The **chip** 3 and the circuit board 4 are facing to each other and an irregular end plane of the **solder columns** 6 are engaged with each other. Next, the low-melting-point solder 2 coating said end planes of the **solder columns** 6 is locally heated and fused to connect the planes. Accordingly, positioning of the **chip** 3 and the circuit board 4 is performed steadily and the

connection in which deterioration due to heat of the **chip** 3 is prevented becomes possible.

L42 ANSWER 36 OF 36 JAPIO COPYRIGHT 2002 JPO
AN 1986-208226 JAPIO
TI WIRING BOARD FOR MOUNTING SEMICONDUCTOR ELEMENT
IN KUWASHIMA HIDEJI; KAMIYAMA MAMORU; NAKANO NAOKI
PA HITACHI CHEM CO LTD, JP (CO 000445)
PI JP 61208226 A 19860916 Showa
AI JP1985-49053 (JP60049053 Showa) 19850312
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 478, Vol. 11, No. 41, P. 108 (19870206)
AB PURPOSE: To obtain a wiring board with excellent dielectric constant, efficient heat conductivity and heat radiation for mounting a semiconductor element by a method wherein a heat conduction plate which is isolated from a conductive circuit and a conductive layer and which has a flat part on its top is provided in a large piercing hole drilled in a substrate and the semiconductor element is mounted on the flat part of the heat conduction plate.
CONSTITUTION: A semiconductor element 11 is mounted on a mother **chip** 10 and welded by a **solder column** to form a compound semiconductor element. The compound semiconductor element is bonded onto a protrusion 8 of a heat conduction plate 7 with liquid silicon rubber. Wire bonding terminals on the mother **chip** 10 and wire bonding terminals on a semiconductor element mounting wiring board which has nail head pins 9 stuck in small piercing holes 1 drilled in it are connected to each other with aluminum wires 12 by ultrasonic welding. The 72 nail head pins 9 exposed from the semiconductor element mounting wiring board are inserted into a no-load insertion socket and then held to fix in the socket by the manipulation of a lever.

L43 ANSWER 1 OF 1 WPIX (C) 2002 THOMSON DERWENT
AN 2001-411107 [44] WPIX
DNN N2001-304194 DNC C2001-124588
TI Column grid array connector to establish a connection between an electrical connector and a substrate comprises a mounting housing, electrical contact terminals and **solder columns**.
DC L03 M23 V04 X24
IN HARPER, D K
PA (BRGL) BERG ELECTRONICS MFG BV; (BRGL) BERG TECHNOLOGY INC; (FCIA-N) FCI AMERICAS TECHNOLOGY INC
CYC 28
PI EP 1111973 A2 20010627 (200144)* EN 14p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR
JP 2001217027 A 20010810 (200154) 9p
US 6353191 B1 20020305 (200224)
ADT EP 1111973 A2 EP 2000-126576 20001212; JP 2001217027 A JP 2000-378698 20001213; US 6353191 B1 US 1999-460008 19991213
PRAI US 1999-460008 19991213
AB EP 1111973 A UPAB: 20011001
NOVELTY - Electrical connector comprises: a housing (3) with mounting surface; electrical contact terminals (5) in the housing; and **solder columns** (8), each of which is attached to a tail, so at least a portion of the tail extends to a predetermined distance into the **solder column**.
DETAILED DESCRIPTION - Each of the contact terminals (5) comprises a tail formed at a **distal** end of the terminal. Each tail passes through and extends from the mounting surface of the housing. The **solder column** is preferably a 90 Pb 10Sn solder alloy.
INDEPENDENT CLAIMS are also included for:
(a) a method of depositing solder about a tail portion of a terminal of an electrical connector; and
(b) the formation of a number of **solder columns**.
USE - For connections to PCBs and other substrates.
DESCRIPTION OF DRAWING(S) - The drawing shows a perspective view of the electrical connector.
housing 3
contact terminals 5
solder columns 8
Dwg.1/8

L45 ANSWER 1 OF 25 WPIX (C) 2002 THOMSON DERWENT
AN 2001-482535 [52] WPIX
DNN N2001-357190 DNC C2001-144567
TI Multilayer interconnection substrate for semiconductor devices, e.g. ball grid array, comprises metal column formed on **terminal** pads and covered with resin film.
DC L03 U11 U14
IN IIJIMA, T; MATSUDA, Y; WAKABAYASHI, S
PA (SHIA) SHINKO DENKI KOGYO KK; (IIJI-I) IIJIMA T; (MATS-I) MATSUDA Y; (WAKA-I) WAKABAYASHI S
CYC 2
PI US 2001008309 A1 20010719 (200152)* 31p
JP 2001196496 A 20010719 (200156) 17p
ADT US 2001008309 A1 US 2000-736864 20001214; JP 2001196496 A JP 2000-4873 20000113
PRAI JP 2000-4873 20000113
AB US2001008309 A UPAB: 20010914
NOVELTY - A multilayer interconnection substrate (211) has an uppermost connection layer having **terminal** pads formed corresponding to external connection **terminals**; a metal column formed on each **terminal** pad; a resin film covering the side surface of the metal column (208); and insulating layer formed on the uppermost interconnection layer so that a gap is formed between the insulating layer and resin film.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for
(A) a method of manufacturing the above multilayer interconnection substrate comprising forming **terminal** pads (203b) and an insulating layer in an uppermost interconnection layer, forming openings in the insulating layer; filling each opening with metal particles; forming a metal column in each opening by melting the metal particles; and removing a portion of insulating layer near but not adjacent the metal column; and
(B) a semiconductor device comprising the above multilayer interconnection substrate, and a semiconductor mounting element (205).
USE - For semiconductor device, e.g. ball grid array.
ADVANTAGE - The metal column relaxes stress caused by different coefficients of thermal expansion on the semiconductor device. The formation of metal column on the interconnect substrate shortens the duration of post-process, thus reducing the possibility of the semiconductor element falling inferior in the post-process.
DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view of a multilayer interconnection substrate.
Terminal pads 203b
Semiconductor mounting element 205
Solder 207
Metal column 208
Multilayer interconnection substrate 211
Dwg.3/17

L45 ANSWER 2 OF 25 WPIX (C) 2002 THOMSON DERWENT
AN 2000-484738 [43] WPIX
DNN N2000-360403 DNC C2000-145981
TI Semiconductor wafer for chip sized semiconductor devices has columnar electrodes with plated tops for bonding to external **terminals**.
DC L03 U11
IN IHARA, Y; KOBAYASHI, T; WAKABAYASHI, S
PA (SHIA) SHINKO ELECTRIC IND CO LTD
CYC 28

PI EP 1024531 A2 20000802 (200043)* EN 22p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
JP 2000216111 A 20000804 (200051) 7p
JP 2000216185 A 20000804 (200051) 9p
KR 2000053618 A 20000825 (200121)
TW 444288 A 20010701 (200220)
ADT EP 1024531 A2 EP 2000-300613 20000127; JP 2000216111 A JP 1999-18229 19990127; JP 2000216185 A JP 1999-18237 19990127; KR 2000053618 A KR 2000-3629 20000126; TW 444288 A TW 2000-101296 20000126
PRAI JP 1999-18237 19990127; JP 1999-18229 19990127
AB EP 1024531 A UPAB: 20000907
NOVELTY - A semiconductor wafer has columnar electrodes (24) connected to wiring lines and with plated tops (41) for bonding to external **terminals**. The wafer is encapsulated except for the tops of the columnar electrodes.
DETAILED DESCRIPTION - A semiconductor wafer comprises columnar electrodes (24) and electrode **terminals** on its surface, an insulation film on which patterned wiring lines (27) are formed which are connected to an electrode **terminal** at one end and to a columnar electrode at the other and an encapsulating layer from which the top of the columnar electrodes are exposed. These electrodes are provided with nickel/nickel alloy (Ni/Ni alloy), palladium and gold films successively plated at their tops (41).
INDEPENDENT CLAIMS are also included for methods of producing the wafer above and for a semiconductor device comprising the wafer above.
USE - Semiconductor wafers for chip-sized packages.
ADVANTAGE - The **columnar** electrodes have increased **solder** wettability, giving firmer bonding to an external **terminal** such as a solder ball and device reliability is increased.
DESCRIPTION OF DRAWING(S) - A section of the semiconductor wafer is shown.
Columnar electrodes 24
Wiring lines 27
Plated films 41
Dwg.3D/12

L45 ANSWER 3 OF 25 WPIX (C) 2002 THOMSON DERWENT
AN 1996-314975 [32] WPIX
DNN N1996-265133
TI Semiconductor device circuit mounting method e.g. for ball grid array package - using conductive column in bump **terminal** compressed to mother-board **terminal** where **column** compression becomes **soldering** joint between bump and mother-board **terminal**.
DC U11
PA (SONY) SONY CORP
CYC 1
PI JP 08139226 A 19960531 (199632)* 5p
ADT JP 08139226 A JP 1994-293695 19941104
PRAI JP 1994-293695 19941104
AB JP 08139226 A UPAB: 19960819
The device has a conductive column (10) which formed in a spring shape in a bump **terminal** (4). The bump **terminal** conductive column is compressed to a motherboard **terminal** (11).
The compression of the conductive column to the motherboard **terminal** with a soldering paste (32) becomes a soldering joint between the bump and motherboard **terminal**.
ADVANTAGE - Provides connection between substrates for long period of

time and enables package connection to other components. Provides superb circuit of semiconductor device with high reliability and improves operation of semiconductor device.
Dwg.1/7

L45 ANSWER 4 OF 25 WPIX (C) 2002 THOMSON DERWENT
AN 1992-361155 [44] WPIX
TI Connecting **terminal** soldering method to **solder** periphery of **column** - conducts **soldering** three times e.g. bottom side, upper side, and total forming NoAbstract.
DC V04 X24
PA (NIEJ) JAPAN ELECTRONIC CONTROL SYSTEM
CYC 1
PI JP 04262385 A 19920917 (199244)* 5p
ADT JP 04262385 A JP 1990-401330 19901211
PRAI JP 1990-401330 19901211

L45 ANSWER 5 OF 25 WPIX (C) 2002 THOMSON DERWENT
AN 1988-099743 [15] WPIX
DNN N1988-075632
TI Solder **terminal** for pinless module - is produced by filling via holes with flux by capillarity, applying solder preform to resulting flux glob, and heating.
DC P55 U11 U14
IN BITAILLOU, A; GRANDGUILL, M J
PA (IBMC) IBM CORP
CYC 6
PI EP 263222 A 19880413 (198815)* EN 10p
R: DE FR GB IT
JP 63098186 A 19880428 (198823)
US 4830264 A 19890516 (198923) 7p
EP 263222 B 19920325 (199213) 10p
R: DE FR GB IT
DE 3684602 G 19920430 (199219)
ADT EP 263222 A EP 1986-430037 19861008; US 4830264 A US 1987-106094 19871007; EP 263222 B EP 1986-430037 19861008
PRAI EP 1986-430037 19861008
AB EP 263222 A UPAB: 19930923
The solder **terminals** for the metallised ceramic module (11) having via holes terminating with eyelets (15) at one surface are formed by applying a drop of flux at the bottom of each via hole to file the latter by capillarity and form a glob (19) at its upper end. A solder preform (20) is then applied to the flux glob, to which it adheres.
Heating thereafter causes solder reflow to fill the via hole and eyelet with solder. The subsequently cooled solder provides a **terminal** which fills the via hole, includes a solder mound (23) making connection with the eyelet, and provides a solder bump (22) at the opposite end of the via hole.
ADVANTAGE - Permits direct mounting of module on printed circuit board.
2/3

L45 ANSWER 6 OF 25 WPIX (C) 2002 THOMSON DERWENT
AN 1983-D1832K [10] WPIX
DNN N1983-041628
TI Control plate for plasma display panel - has glass foil with X and Y-conductors located on either side to minimise short circuits.
DC P85 V05 W05
IN GSCHWANDTN, A

PA (SIEI) SIEMENS AG
CYC 1
PI DE 3132070 A 19830303 (198310)* 8p
PRAI DE 1981-3132070 19810813
AB DE 3132070 A UPAB: 19930925
The control plate of a matrix plasma display panel is in the form of a thin glass foil (e) that has a matrix of holes. Fine conductor wires are laid in a matrix (f,d) on the top and bottom surfaces of the foil in order to produce a matrix of crossover points coinciding with the hole centres.

The line conductors (f) are brought out to soldered strip **terminals** on either side (j) of the panel. **Column** conductors locate with glass **solder** bars (1). By locating the matrix conductors on either side of the foil, the possibility of a short circuit or wire break is minimised.

3/3

L45 ANSWER 7 OF 25 WPIX (C) 2002 THOMSON DERWENT
AN 1982-F7390E [20] WPIX
TI RAM dual slice semiconductor cell - has low melting point galvanic connection between two slices.
DC U13 U14
IN KOHARA, M; NAKATA, H; SHIBATA, H
PA (MITQ) MITSUBISHI ELECTRIC CORP
CYC 2
PI DE 3141056 A 19820513 (198220)* 28p
JP 57071171 A 19820501 (198223)
DE 3141056 C 19880114 (198802)
ADT DE 3141056 A DE 1981-3141056 19811015
PRAI JP 1980-147165 19801020
AB DE 3141056 A UPAB: 19930915
The high integration density semiconductor device includes a dynamic storage cell mos transistor produced on a semiconductor substrate (10). The first group of components on the lower substrate (10) are connected to a second group on a sapphire substrate (60) by a central hump (54,74) of low melting point substance.

The first substrate (10) carries the component parts of an active RAM and the second substrate (60) forms the electrical dielectric and electrode sections of the RAM associated capacitor. The hump (54) of lead or tin, typically is between sintered metal electrodes (50) and is melted to form the required contact shape.

6

L45 ANSWER 8 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 2001-298114 JAPIO
TI BGA PACKAGE AND MOUNTING STRUCTURE OF BGA PACKAGE AND BOARD
IN KAWAMICHI TOMOHISA
PA OKI ELECTRIC IND CO LTD
PI JP 2001298114 A 20011026 Heisei
AI JP2000-112028 (JP2000112028 Heisei) 20000413
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2001
AB PROBLEM TO BE SOLVED: To solve a difficulty of remounting a BGA package on a board when the package is removed from the board.
SOLUTION: An external **terminal** of a semiconductor element 1 of the BGA package is formed of a **columnar** pin 7 and a **solder** ball 8 covering a periphery of the pin 7.
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L45 ANSWER 9 OF 25 JAPIO COPYRIGHT 2002 JPO

AN 2001-284381 JAPIO
TI SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE
IN TAKAO YUKIHIRO
PA SANYO ELECTRIC CO LTD
PI JP 2001284381 A 20011012 Heisei
AI JP2000-092688 (JP2000092688 Heisei) 20000330
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2001
AB PROBLEM TO BE SOLVED: To enhance reliability at mounting of a chip size package.
SOLUTION: A columnar **terminal** 9 having constricted side face, where the area of upper surface is larger than the area of bottom face, is formed and a solder ball 12 is mounted thereon. Since the contact area S of the **columnar terminal** 9 and the **solder** ball 12 can be increased, as compared with a conventional one, strength against shearing stress can be enhanced. Furthermore, constricted shape reduces rigidity (makes flexible) and increases resiliency thus enhancing stress relaxing performance.

L45 ANSWER 10 OF 25 JAPIO
AN 2001-006656 JAPIO
TI **TERMINAL** FOR STORAGE BATTERY
IN TOGA TAKAYOSHI
PA KYOCERA CORP
PI JP 2001006656 A 20010112 Heisei
AI JP1999-180386 (JP11180386 Heisei) 19990625
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2001
AB PROBLEM TO BE SOLVED: To join an insulated base with a **terminal** column always strongly without generating cracking in the insulated base.
SOLUTION: A **terminal** for a storage battery is structured so that a **terminal** column 2 is inserted to inside an insulated base 1 in cylindrical shape made of ceramics and **brazed** fast. The **terminal column** 2 is composed of a cylindrical member 2a made of one of the aluminum, aluminum alloy, copper and copper alloy and a stress relieving member 2b in rod shape installed inside the cylindrical member 2a and having a smaller coefficient of thermal expansion than the cylindrical member 2a. When the base 1 and **terminal column** 2 are **brazed** together, stress generated between them will remain small, and the base 1 can be precluded from crack initiation.

L45 ANSWER 11 OF 25 JAPIO
AN 1999-126863 JAPIO
TI WIRING BOARD AND PRODUCTION THEREOF
IN MATSUURA TORU
PA NGK SPARK PLUG CO LTD, JP (CO 000454)
PI JP 11126863 A 19990511 Heisei
AI JP1997-292715 (JP09292715 Heisei) 19971024
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 99, No. 5
AB PURPOSE: TO BE SOLVED:To provide a wiring board having **terminals** which ensure high connection reliability, and a production method therefor.
CONSTITUTION: substantially planar wiring board 10 having first and second faces 1a, 1b comprises a wiring board body 1 made of a composite material of epoxy resin and glass fibers, an integrated circuit chip 11 mounted on the first face 1a side, and substantially cylindrical columnar **terminals** 3 made of Pb-Sn eutectic solder having a height CH

larger than the maximum diameter AD formed on the second face 1b side. When the forward end of the columnar **terminal** 3 is abutted against a fixing pad formed on a fixing board and connected by a **solder**, the **columnar terminal** 3 is bent for a deformation along the second face and elongates/contracts for a deformation caused by the difference in the coefficients of thermal expansion between the integrated circuit chip 11 and the wiring board body 1. Consequently, stress is relaxed, and the columnar **terminal** is not ruptured easily thus enhancing the connection reliability.

L45 ANSWER 12 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1998-163365 JAPIO
TI SEMICONDUCTOR PACKAGE AND MOUNTED CIRCUIT DEVICE
IN NAGANO JUNYA
PA TOSHIBA CORP, JP (CO 000307)
PI JP 10163365 A 19980619 Heisei
AI JP1996-318222 (JP08318222 Heisei) 19961128
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 98, No. 6
AB PURPOSE: TO BE SOLVED:To avoid short-circuiting between adjacent connected points due to deformation of solder bumps to facilitate performing a high reliability mounting/ connecting work by making circular **columnar** the **solder** bumps on external connection **terminal** surfaces and equalizing the solder heights at the solder bump bond zones. CONSTITUTION: semiconductor package comprises a board 17 having external connection **terminals** 9a and semiconductor devices which are mounted on other main surface of the board 17 and electrically connected corresponding to these **terminals** 9a. A support base 15 of the board 17 is disposed at the outgoing side of the **terminals** 9a, insulated and distant from circular **columnar solder** bumps 14 and the **terminals** 9a. While the external connection **terminals** 9a and conductive pads 17a of the board 17 are connected, the weight of the semiconductor package 16 is supported by the base 15 enough to suppress the solder bumps 14 from deforming or sinking, thus avoiding the short circuit.

L45 ANSWER 13 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1998-125726 JAPIO
TI SUBSTRATE AND ITS CONNECTION
IN OKA KOICHI
PA FUJI XEROX CO LTD, JP (CO 359761)
PI JP 10125726 A 19980515 Heisei
AI JP1996-277908 (JP08277908 Heisei) 19961021
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 98, No. 5
AB PURPOSE: TO BE SOLVED:To provide a substrate which can beforehand prevent breaking of a connection part caused by a concentrated stress, by shaping connected bumps reliably into such a predetermined configuration as to avoid any concentrated stress, and also to provide a method for connecting the substrate.
CONSTITUTION: t, as shown in the drawing (A), an IC chip 10 having **terminal** electrode parts 11 and **columnar** bumps 12C of **solder** formed on the electrode parts 11 is positioned above **terminal** electrode parts 18 of a circuit substrate 16 with the side of the bumps 12C facing down, the bumps 12C are heated to be melted by reflow, the entire IC chip 10 is moved in an arrowed direction 30 until the surface of a protective film 14 covering a **terminal** electrode 11 side of the chip 10 come into contact with the surface of a protective film 20 on the circuit substrate 16, and then the bumps 12C are

cooled and fixedly set. As a result, as shown in the drawing (B), the bumps 12C are changed to drum-shaped bumps 12D having the same shape as openings 22 made in the protective film 20.

L45 ANSWER 14 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1996-203021 JAPIO
TI PRODUCTION OF MAGNETIC HEAD
IN MASUDA KENZO; SHIINA HIROMI; OIKAWA GEN; IMANAKA RITSU
PA HITACHI LTD, JP (CO 000510)
HITACHI KYOWA KOGYO CO LTD, JP (CO 485527)
PI JP 08203021 A 19960809 Heisei
AI JP1995-8305 (JP07008305 Heisei) 19950123
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 96, No. 8
AB PURPOSE: To form high-reliability take-out electrodes on the side end face different from an end face having a magnetic conversion element without largely changing the stages of a process for producing conventional type magnetic head.
CONSTITUTION: The high-reliability take-out electrode 13 is led out by forming the lower **terminal** of the conventional type magnetic head by Au or **solder** material into a **columnar** shape and cutting out a slider in a position along the lower **terminal** where the lead electrode 2 is not exposed. The high-reliability take-out electrode 13 is assured at the side end face different from the end face provided with the magnetic conversion element and a contribution is made to miniaturize the magnetic head slider. This process is attained only by the minor change of the process for producing conventional type magnetic head.

L45 ANSWER 15 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1995-218926 JAPIO
TI DISPLAY DEVICE
IN TAMURA MASANORI; YAMASHITA OSAMU; ISOBE MASAYOSHI
PA SANYO ELECTRIC CO LTD, JP (CO 000188)
TOTTORI SANYO ELECTRIC CO LTD, JP (CO 323436)
PI JP 07218926 A 19950818 Heisei
AI JP1994-11085 (JP06011085 Heisei) 19940202
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 95, No. 8
AB PURPOSE: To surely connect a substrate and a driving element even when the electrode of a **terminal** part is damaged by connecting both the **terminals** with a specified connecting agent between the substrate of a display and the respective **terminal** parts of the driving element.
CONSTITUTION: A substrate 1 of a liquid crystal display or the like is exposed on the surface of a pedestal 11 of a glass panel or the like, composed of a transparent electrode and equipped with a **terminal** part (area) 2 arranged with **terminals** 12 in a line. On the other hand, a driving element 3 for driving a display such as the liquid crystal display is provided with an integrated circuit element 32 in a film-shaped supporter 31 and arranged with **terminal** part electrodes 33 in a line composed of a tongue-shaped metal foil set body such as copper foil. Further, an adhesive 4 generally called anisotropic conductive material is mixed with an adhesive resin agent so as to obliquely arrange the **column** of **soldering** particles and by applying pressure in a direction of thickness, electric conduction is provided in the direction of thickness but no electric conduction is provided in a breadthwise direction, namely, in a direction of a plane crossing the direction of thickness. Then, the **terminal** part 2 is connected

through the connecting agent 4 to the **terminal** part electrodes 33 of the driving element.

L45 ANSWER 16 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1992-262385 JAPIO
TI **TERMINAL** SOLDERING METHOD
IN MOGI YOSHIHISA; KATSURAGAWA FUKUMI
PA JAPAN ELECTRON CONTROL SYST CO LTD, JP (CO 470862)
PI JP 04262385 A 19920917 Heisei
AI JP1990-401330 (JP02401330 Heisei) 19901211
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1313, Vol. 17, No. 47, P. 109 (19930128)
AB PURPOSE: To **solder** a **columnar** connection **terminals** having a relatively large dia. certainly by performing at least three soldering motions repeatedly while a proper amount of solder is supplied.
CONSTITUTION: The periphery of a **columnar** connection **terminal** is **soldered** to the upper part of a **terminal** 21 using a soldering iron 1. The iron 1 is pressed to the joining part of connection **terminals** 11a, 12a and the **terminal** 21 with each other from above at least in three repetitive soldering motions. At the first pressing of the iron 1, a specified amount of solder is supplied to the joining part, and more solder is supplied at the time of second pressing. At the time of the third pressing of iron and thereafter, less solder than in the second soldering motion is supplied.

L45 ANSWER 17 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1991-036614 JAPIO
TI CIRCUIT MODULE
IN OKADA ISAO; KATO YOSHIYUKI; IDE KOJI; YASUMA TOSHIHIKO; RICHIYAADO JII GAIGAA; AKIO TANAKA; SADA RYUICHI; BABA MIKITO
PA MITSUMI ELECTRIC CO LTD, JP (CO 000622)
PI JP 03036614 A 19910218 Heisei
AI JP1989-171715 (JP01171715 Heisei) 19890703
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: P, Sect. No. 1197, Vol. 15, No. 172, P. 113 (19910430)
AB PURPOSE: To efficiently secure the mounting area of semiconductor parts by widening an area for providing a **terminal** and to miniaturize a substrate by providing the **terminal** of the semiconductor parts assembled to the substrate on plural sides of the outer peripheral side.
CONSTITUTION: Each pin **terminal** 58 is provided in a state that its part protruded to the upper part is inserted into a through-hole of a substrate 31 and **soldered**, and **columnar** blocks 54 - 57 which are made of a synthetic resin and whose cross section is roughly rectangular abut on the lower face 31b along the periphery of the substrate 31. Accordingly, even if the substrate 31 is small, many **terminals** can be provided, and also, an area where semiconductor parts can be mounted can be secured efficiently on the substrate 31, therefore, the substrate 31 can be miniaturized.

L45 ANSWER 18 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1990-060051 JAPIO
TI HERMETICAL FORMATION OF STORAGE BATTERY **TERMINAL** PORTION
IN ISHIKAWA YUKITSUGU
PA FURUKAWA BATTERY CO LTD:THE, JP (CO 000538)
PI JP 02060051 A 19900228 Heisei
AI JP1988-211136 (JP63211136 Heisei) 19880825
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No.

928, Vol. 14, No. 229, P. 83 (19900515)
AB PURPOSE: To prevent a tubular insulating material located around the outer periphery of a columnar core member from being cracked due to thermal expansion of the core member by applying a thin layer of wax on the bottom face of an upwardly open columnar recessed hole provided through a battery lid and surrounded by tubular walls, and loading the columnar core member in the hole and thermally soldering them to each other.
CONSTITUTION: A bottomed tubular polar column 11 which has a columnar recessed hole open at its upper side is soldered with 8 to a tubular inorganic insulating material 4, which is soldered with 7 to an annular sealing material 5 welded to a **terminal** polar column insertion hole 3 formed through a battery lid 2; the polar column being tubular, its thermal expansion D is so small in its radial direction that the insulating material 4 is not cracked thereby. Next, a columnar core member 13 is loaded in the recessed hole of the polar **column** 11 and is thermally **soldered** thereto by means of a thin layer of wax material 12 applied on the bottom face of the hole; since the core member is separated from the tubular wall of the column 11, even when thermally expanded, it does not exert expansive forces on the insulating material 4 located around its outer periphery so that the material is prevented from being cracked.

L45 ANSWER 19 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1990-054861 JAPIO
TI HERMETICAL FORMING METHOD FOR STORAGE BATTERY **TERMINAL** SECTION
IN ISHIKAWA YUKITSUGU; TOGA TAKAYOSHI
PA FURUKAWA BATTERY CO LTD:THE, JP (CO 000538)
KYOCERA CORP, JP (CO 358923)
PI JP 02054861 A 19900223 Heisei
AI JP1988-204245 (JP63204245 Heisei) 19880817
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 926, Vol. 14, No. 222, P. 7 (19900510)
AB PURPOSE: To prevent the occurrence of cracks on a circular inorganic insulating material and obtain a **terminal** section with stable airtightness by forming a **terminal** electrode pole into a bottomed cylindrical electrode pole and brazing its cylindrical wall and the cylindrical inorganic insulating material on the outer periphery.
CONSTITUTION: An inorganic cylindrical electric insulating material 4 is inserted into a space between a **terminal** cylindrical electrode pole 1 and a cover hole peripheral wall 2a, and the outer periphery of the insulating material 4 and the inner periphery end 5b folded downward in a U-shape of a metallic flange 5 are airtightly brazed 7 and seal-bound. The outer periphery of the electrode pole 1 and the inner periphery of the insulating material 4 on its outer periphery are **brazed** and bound. A metallic **column**-shaped core member 12 with the diameter slightly smaller than the inner diameter of a cylindrical wall 1b is inserted into the columnar recessed hole 11 of the electrode pole 1 at a gap 11a, a wax material 13 is filled in the gap 11a, the member 12 and the inner periphery of the cylindrical wall 1b are brazed 13 over the whole length of the height, and a solid electrode pole **terminal** 14 is obtained.

L45 ANSWER 20 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1989-258356 JAPIO
TI CONSTITUTION METHOD FOR AIRTIGHT **TERMINAL** PART OF STORAGE BATTERY
IN ISHIKAWA YUKITSUGU
PA FURUKAWA BATTERY CO LTD:THE, JP (CO 000538)
PI JP 01258356 A 19891016 Heisei

AI JP1988-85580 (JP63085580 Heisei) 19880407
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 871, Vol. 14, No. 12, P. 155 (19890111)
AB PURPOSE: To prevent the fracture of a circular insulation member due to tensile stress generated during a direct brazing process and enhance the performance of airtightness, liquid leakage resistance, mechanical strength and the like by **brazing** tightly a **terminal** polar **column** passing the metal vessel wall of a battery to the external circular insula tion member thereof via a circular metal member. CONSTITUTION: A hole 3 is vertically made through the battery lid wall 2 of a metal vessel for an airtight battery A and a polar column 1 is fitted while the upper end thereof is projected externally. An inorganic circular insulation member 4 is provided on the external surface of the polar column 1 for the electrical insulation of a space between the column 1 and the internal peripheral wall part of a lid wall 2 forming the enclosure of the aforesaid hole 3. Furthermore, the polar column 1 and the member 4 are seal connected to each other by the heating and deposition of a brazing material 6 via the circular metal member 5 of the predetermined thickness, thereby obtaining an airtight **terminal** part (a). According to the aforesaid construction, the thermal expansion and contraction of the polar column 1 can be absorbed by the member 5 and, therefore, it is possible to prevent the fracture of the member 4 and obtain the **terminal** of high airtightness.

L45 ANSWER 21 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1988-315261 JAPIO
TI THERMAL RECORDING HEAD
IN MEGO KAZUYOSHI; SAKASHITA YASUYUKI
PA HITACHI LTD, JP (CO 000510)
PI JP 63315261 A 19881222 Showa
AI JP1987-151120 (JP62151120 Showa) 19870619
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: M, Sect. No. 814, Vol. 13, No. 154, P. 42 (19890414)
AB PURPOSE: To achieve improvement of connection reliability of a soldering part, by a method wherein dummy **terminals** other than soldering **terminals** are provided between a flexible print plate (FPC) and a substrate of a different coefficient of thermal expansion to be soldered thereto, and a solder height after connection is controlled. CONSTITUTION: A soldered connection **terminal** 4 which is circuit formed by a thin film process and a dummy **terminal** 6 which is formed by a thick film process are provided between FPC1 and a head substrate 3 which are different in coefficient of thermal expansion. Then, after registering of the soldered FPC1 side **terminal** to a connection **terminal** 4 formed on the head substrate 3 side, soldering connection is performed by thermal pressure contact with a hot ram. In that case, since a dummy **terminal** 6 for regulation of height formed by a thick film is provided between the substrate 3 and the FPC1, a solder height of a connection part after solder fusion can be controlled by a film thickness of the dummy **terminal** 6 served doubly as a spacer. Therefore, high connection reliability can be obtained by a **columnar solder** 5 formed between a connection **terminal** 2 and the connection **terminal** 4.

L45 ANSWER 22 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1988-157638 JAPIO
TI **TERMINAL** PART OF ENCLOSED TYPE LEAD ACCUMULATOR AND ITS MANUFACTURE
IN OGUMA MIKIO; KOMAKI AKIO; HIRONAKA KENSUKE; WADA YASUNAO; MATSUBAYASHI SATOSHI; OKURA TOMOYUKI; YAMANA TAKUMI; YABUI YOSHIMI; AOKI MASAYOSHI;

TAKASU MASATOSHI
PA SHIN KOBE ELECTRIC MACH CO LTD, JP (CO 000120)
PI JP 63157638 A 19880630 Showa
AI JP1986-303494 (JP61303494 Showa) 19861219
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 679, Vol. 12, No. 42, P. 108 (19881108)
AB PURPOSE: To obtain a sufficient mechanical strength without exposing a pole column member to the outside by joining an eyelet-like **terminal** member to said pole column member and then insert-molding said members.
CONSTITUTION: An eyelet-like **terminal** member 1 is caused to fit to the head of a pole column member 3 made of lead or lead alloy until said **terminal** member 1 hits an annular protrusion 12 provided in said pole **column** member 3. Then, **solder** is supplied by a soldering iron 9 from a hole 13 in the head of said **terminal** member 1 to join the **terminal** member 1 and pole column member 3 into an integral body. After that, said integral body is insert-molded by thermoplastic synthetic resin 5 to be formed into a **terminal** part. In this manner, the pole column member 3 made of lead or lead alloy is covered with the eyelet-like **terminal** member 1 made of brass or the like and insert-molded by synthetic resin. Therefore, a sufficient strength can be obtained and there is so possibility that said **terminal** part is worn into powder, then scattering even if it is repeatedly mounted and dismounted.

L45 ANSWER 23 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1986-208226 JAPIO
TI WIRING BOARD FOR MOUNTING SEMICONDUCTOR ELEMENT
IN KUWASHIMA HIDEJI; KAMIYAMA MAMORU; NAKANO NAOKI
PA HITACHI CHEM CO LTD, JP (CO 000445)
PI JP 61208226 A 19860916 Showa
AI JP1985-49053 (JP60049053 Showa) 19850312
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 478, Vol. 11, No. 41, P. 108 (19870206)
AB PURPOSE: To obtain a wiring board with excellent dielectric constant, efficient heat conductivity and heat radiation for mounting a semiconductor element by a method wherein a heat conduction plate which is isolated from a conductive circuit and a conductive layer and which has a flat part on its top is provided in a large piercing hole drilled in a substrate and the semiconductor element is mounted on the flat part of the heat conduction plate.
CONSTITUTION: A semiconductor element 11 is mounted on a mother chip 10 and welded by a **solder column** to form a compound semiconductor element. The compound semiconductor element is bonded onto a protrusion 8 of a heat conduction plate 7 with liquid silicon rubber. Wire bonding **terminals** on the mother chip 10 and wire bonding **terminals** on a semiconductor element mounting wiring board which has nail head pins 9 stuck in small piercing holes 1 drilled in it are connected to each other with aluminum wires 12 by ultrasonic welding. The 72 nail head pins 9 exposed from the semiconductor element mounting wiring board are inserted into a no-load insertion socket and then held to fix in the socket by the manipulation of a lever.

L45 ANSWER 24 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1985-170156 JAPIO
TI LEAD STORAGE BATTERY
IN ONODA YUKIHIRO; SUGIYAMA HIROSHI; KOIKE KIICHI; KOBAYASHI YOSHIHIRO
PA MATSUSHITA ELECTRIC IND CO LTD, JP (CO 000582)
PI JP 60170156 A 19850903 Showa

AI JP1984-25431 (JP59025431 Showa) 19840214
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 372, Vol. 1, No. 5, P. 113 (19860110)
AB PURPOSE: To enhance airtightness and liquid-tightness, and besides to prevent occurrence of corrosion, of a lead storage battery, by attaching a battery jar cover to a lead or lead-alloy electrode-**column**, whose surface is **solder**-plated beforehand.
CONSTITUTION: In case that a lead-alloy electrode-column 1 is attached to a battery jar cover 3 of synthetic resin by adhesive 2, the surface of the electrode **column** 1 is **solder**-plated 6 beforehand. For example, in case that the electrode column 1 of lead-alloy including calcium of 0.1wt% and tin of 1.0wt% is stuck to the battery jar cover 3 of acrylonitrile-butadiene-styrene series synthetic resin by epoxy series adhesive 2, the surface of the **terminal** electrode column 1 is plated 6 in thickness of several hundred .mu.m by solder including tin of 60wt% beforehand. As a solder-plating method, the **terminal** electrode column 1 is dipped in fused solder including tin of 60wt% for several seconds. In this case, it is desirable that the lead oxide film on the surface of the electrode column is removed by lapping prior to solder-plating.

L45 ANSWER 25 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1984-189070 JAPIO
TI AUTOMATIC SOLDERING DEVICE
IN KURODA TORU
PA MATSUSHITA ELECTRIC IND CO LTD, JP (CO 000582)
PI JP 59189070 A 19841026 Showa
AI JP1984-51492 (JP59051492 Showa) 19840316
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: M, Sect. No. 362, Vol. 9, No. 551, P. 17 (19850309)
AB PURPOSE: To provide a titled automatic soldering device which performs automatic soldering in soldering a printed wiring board by rising a molten solder tank when a holder of a horizontal conveyor in which the wiring board is placed comes to a prescribed position.
CONSTITUTION: A holder 16 in which the brazing surface of a printed wiring board 15 inserted therein with the **terminals** of electronic parts is exposed downward arrives to a prescribed position according to the movement of a horizontal conveyor 17. A microswitch 18 is tripped by the holder and a motor 10 is run to rotate a screwed supporting **column** 4 thereby rising a **solder** bath tank 12. When molten solder 13 wets the soldering parts of the board 15 to solder said parts, a contact piece 19 contacts the solder 13 and emits a signal for conducting electricity, by which the motor 10 is run reverse to lower the tank 12. Since only the tank 12 is vertically moved, the mechanism is extremely simple and the automatic soldering device having high accuracy is obtd.